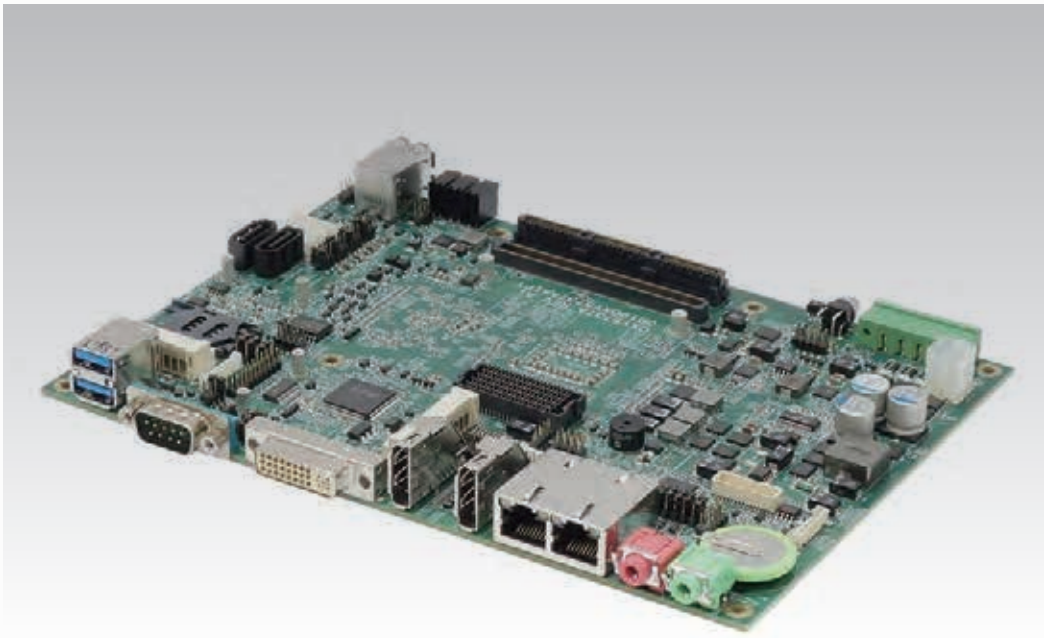
# OXY5737A

## Intel® QM87 EBX SBC
## User's Manual



## Safety Information

**1. Electrical safety**

- To prevent electrical shock hazard, disconnect the power cable from the electrical outlet before relocating the system.
- When adding or removing devices to or from the system, ensure that the power cables for the devices are unplugged before the signal cables are connected. If possible, disconnect all power cables from the existing system before you add a device.
- Before connecting or removing signal cables from the motherboard, ensure that all power cables are unplugged.
- Seek professional assistance before using an adapter or extension cord. These devices could interrupt the grounding circuit.
- Make sure that your power supply is set to the correct voltage in your area.
- If you are not sure about the voltage of the electrical outlet you are using, contact your local power company.
- If the power supply is broken, do not try to fix it by yourself. Contact a qualified service technician or your local distributor.

**2. Operation safety**

- Before installing the motherboard and adding devices on it, carefully read all the manuals that came with the package.
- Before using the product, make sure all cables are correctly connected and the power cables are not damaged. If you detect any damage, contact your dealer immediately.
- To avoid short circuits, keep paper clips, screws, and staples away from connectors, slots, sockets and circuitry.
- Avoid dust, humidity, and temperature extremes. Do not place the product in any area where it may become wet.
- Place the product on a stable surface.
- If you encounter any technical problems with the product, contact your local distributor

## Statement

## Revision History

| Revision | Date (yyyy/mm/dd) | Changes |
|---|---|---|
| Version 1.0 | 2014/09/30 | Initial release |
| Version 1.1 | 2014/10/15 | BIOS function PCH IO configuration |
| Version 1.2 | 2015/07/13 | Change COM1 RS232/422/485 default setting from Loopback to RS232 (JV3, JV2) |
| | | Correct JV4 function |
| | | Correct JP12 jumper setting |
| | | Change COM2 RS232/422/485 default setting from Loopback to RS232 (JV7, JV6) |
| | | Modify LAN1 chipset |
| | | Add JPEG1, JPEG2, JPEG4, J3, JP17, JP18, JP19, JP22, JP20, JP21 jumper setting |
| Version 1.3 | 2016/06/24 | Align sequence of Chapter 2 |
| Version 1.4 | 2016/07/20 | Correct COM1, COM2 and photos of jumpers. |

## Packing list

- ☐ OXY5737A EBX
- ☐ CD (Driver + user's manual)

## Optional Accessories

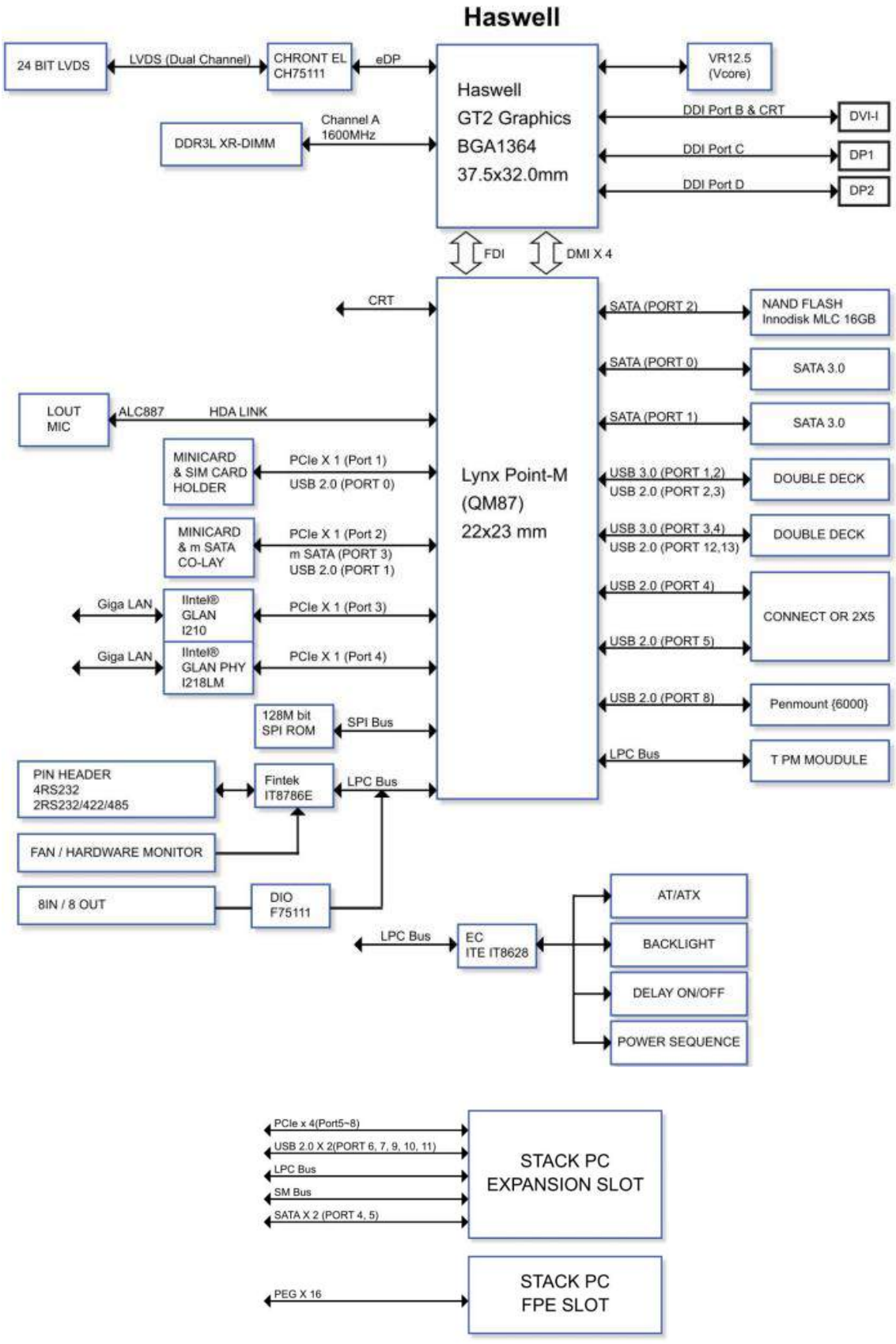
- 1 x Terminal block
- Cable kit for OXY5737A: 1 x SATA, 1 x SATA power, 2 x COM

**If any of the above items is damaged or missing, please contact your local distributor.**

## Table of Contents

# Chapter 1: Product Information

## 1.1 Block Diagram



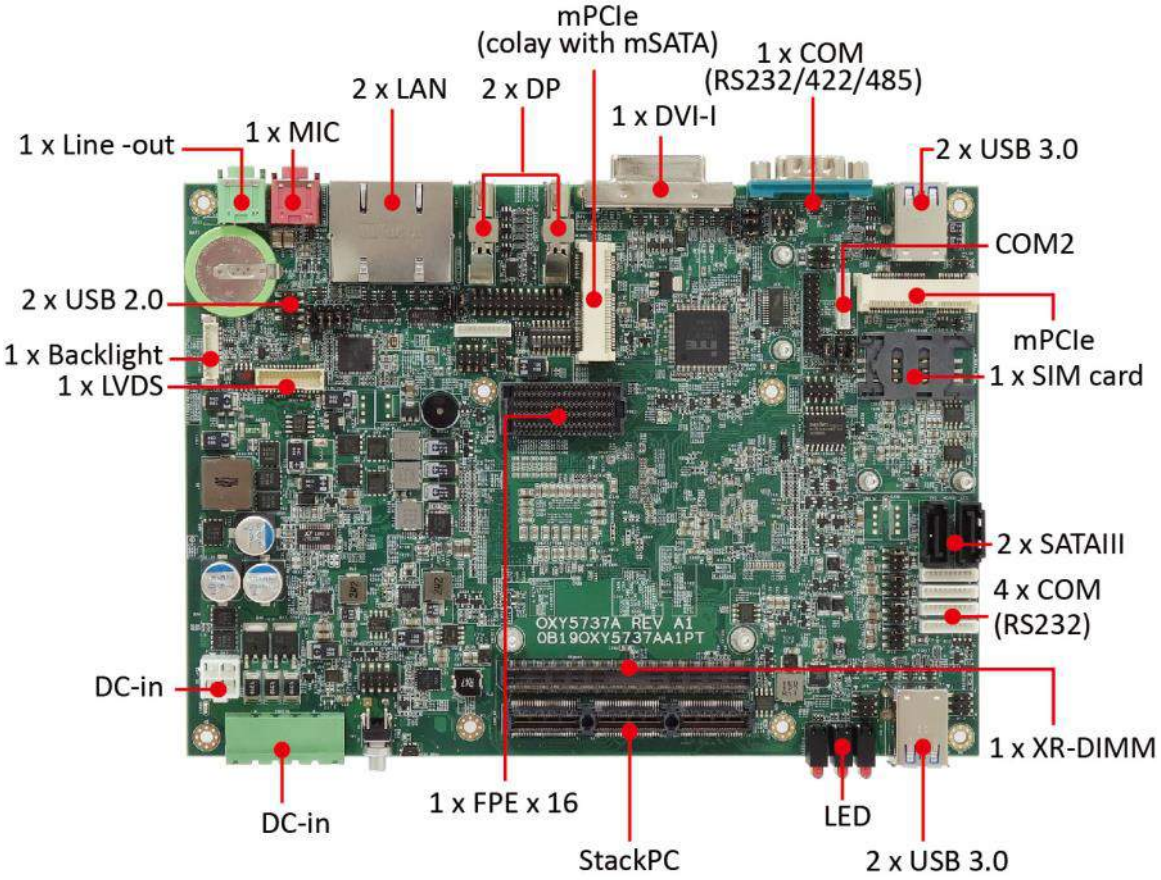
### 1.2 Key Features

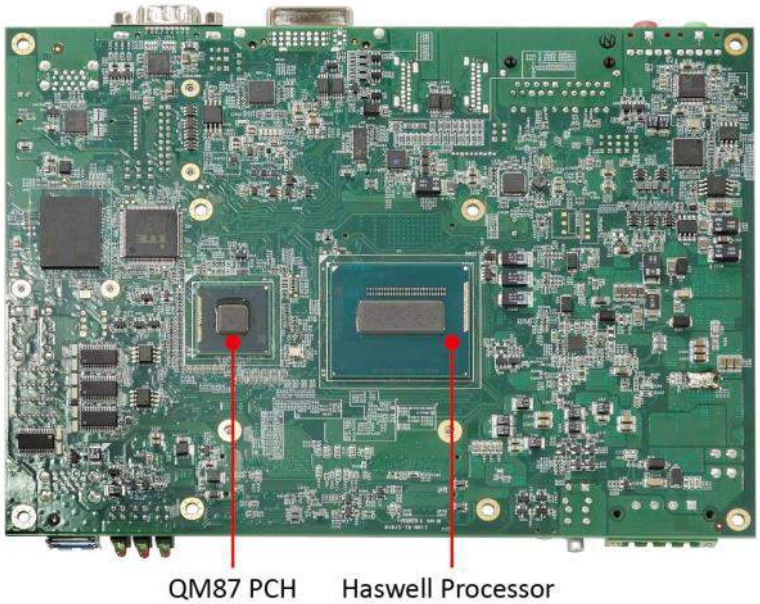
| | |
|---|---|
| System | |
| CPU Type | Intel® Haswell Core™ i7/i3, BGA type<br>Core i7-4700EQ (4C x 2.4/1.7GHz), 6M Cache, (47W/37W)<br>Core i3-4102E (2C x 1.6 GHz), 3M Cache (25W)<br>Celeron 2000E (2C x 2.2 GHz), 2M Cache (37W) |
| Chipset | Intel® Haswell QM87 PCH |
| Memory Type | 1 x DDR3 1600 XR-DIMM up to 8 GB with ECC |
| BIOS | AMI® UEFI BIOS |
| Supoer I/O | ITE8786 |
| Watchdog | 1-255 sec. or 1-255 min. software programmable<br>can generate system reset |
| Expansion Slot | 2 x mPCIe (1 x SIM card, 1 x colay with mSATA) |
| Display | |
| Chipset | Integrated GFX in Haswell processor |
| DVI-I | Yes (Max. resolution 2048 x 1536) |
| LVDS | Dual channel 24-bit LVDS |
| Display Type | 2 x DP, LVDS, DVI-I (DVI-D+VGA) |
| Audio | |
| Codec | Realtek ALC887 High Definition Audio Codec |
| Ethernet | |
| Chipset | Intel® I210-IT & I217-LM GbE |
| WOL | Yes |
| Boot from LAN | Yes for PXE |
| Rear I/O | |
| DP | 1 |
| DVI-D | 1 |
| Ethernet | 2 x RJ45 |
| COM Port | 1 x RS232/422/485 with 5V/12V selectable |
| USB | 2 x USB 3.0 |
| Audio | 1 x MIC, 1 x Line out |
| Power Connector | 1 (Terminal Block) |
| Internal I/O | |
| Touch Panel | 1 x 5-pin |
| Front Panel | 1 (2 x 5-pin) |
| Smart Fan | 1 x CPU Fan, 1 x System Fan |
| Power Connector | 2 (1 x 4-pin/ 2 x 2-pin) |
| SATA | 2 x SATAIII (6 Gb/s) |
| USB | 2 x USB 2.0 by pin header |
| COM | 5 x COM ports: 4 x RS232, 1 x RS232/422/485,<br>all with 5V/12V selectable |
| LVDS | 2 x 15-pin |
| DIO | 2 x 10-pin, 8 in/8 out with isolation |
| SIM card holder | 1 |

| Power Requirements | |
|---|---|
| Input Voltage | 9 to 36 VDC (4-pin terminal block for V+, V+, V-, V-) |
| Power Consumption | without LVDS output |
| With No Load on 4 USB ports | 4A@9VDC, 45W<br>1.6A@24VDC, 45W<br>1.1A@36VDC, 45W |
| With Full Load on 4 USB Ports | 5A@9VDC, 45W<br>1.875A@24VDC, 45W<br>1.25A@36VDC, 45W |
| Mechanical and Environment | |
| Form Factor | EBX |
| Power Type | 9V to 36V DC-in, AT/ATX mode supports with power delay on/off |
| Dimension | 203 x 146 mm (5.75" x 8") |
| Operating Temp. | -40 to 85°C |
| Storage Temp. | -40 to 85°C |
| Relative Humidity | 10% to 90%, non-condensing |

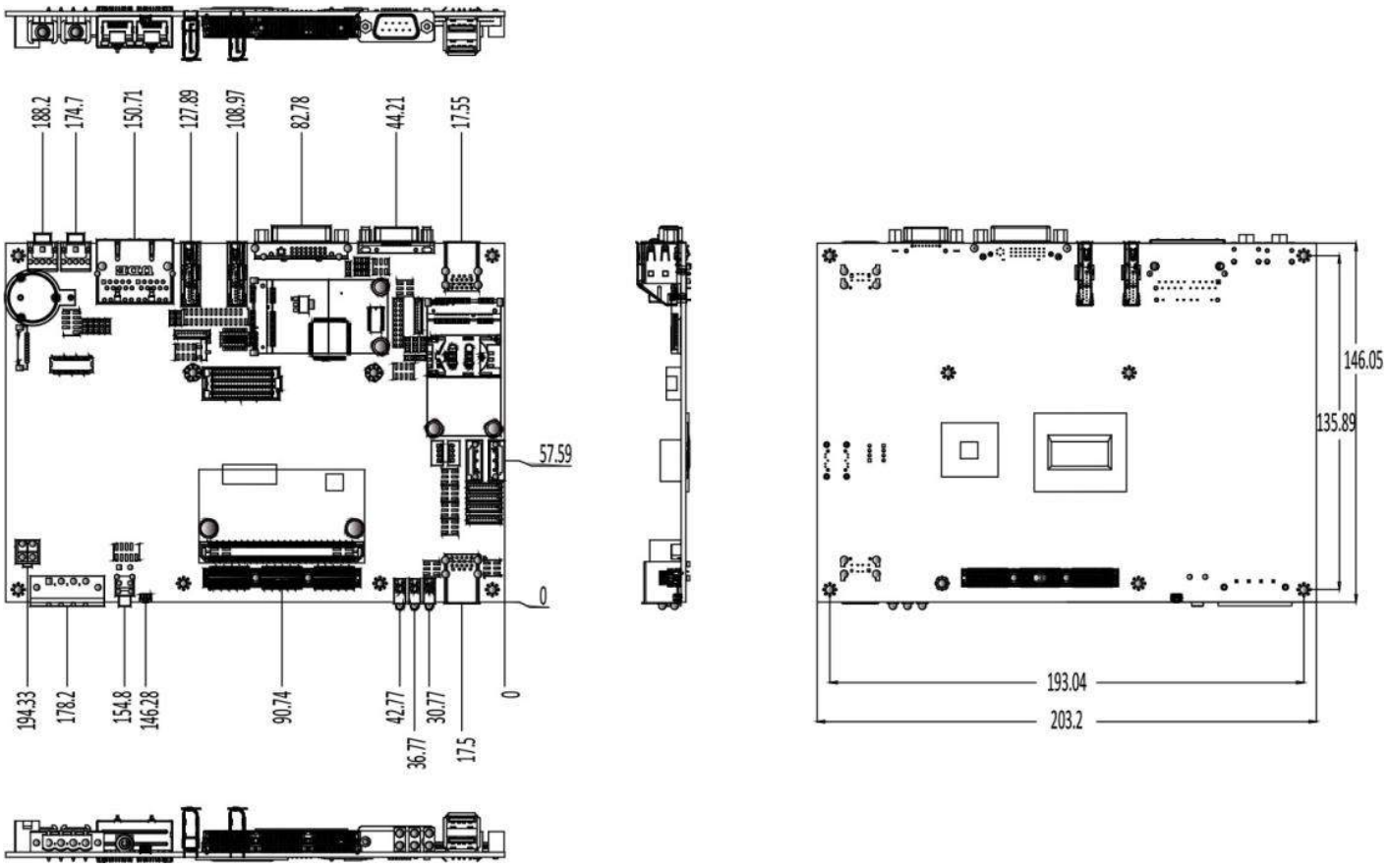
***All specifications and photos are subject to change without notice.**

### 1.3 Board Placement



**1.4 Mechanical Drawings**



## Chapter 2: Jumper, Connector, Switch and LED indicator

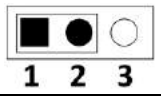
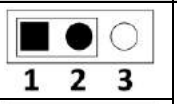
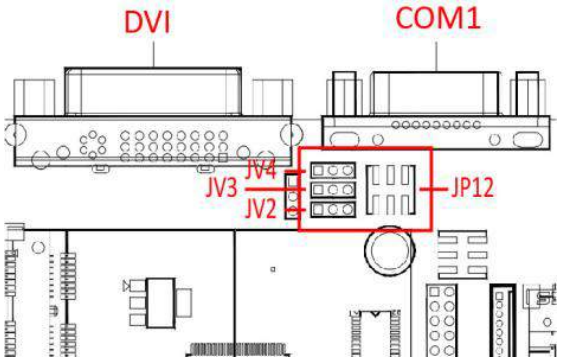
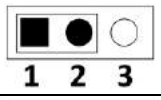
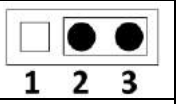
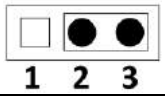
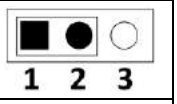
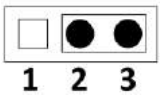
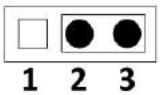
### 2.1 Jumpers and connectors list

| Label | Function |
|---|---|
| BAT1 | BATTERY connector |
| DIMMA1 | DDR3 XR-DIMM Socket |
| LVDS1 | LVDS CONNECTOR |
| MCARD1 | Mini PCIE Card Slot<COLAY M SATA> |
| MINI MPCIE | Mini PCIE Card Slot |
| SATA-CON CN3 | Serial ATA Connectors |
| SATA-CON CN5 | Serial ATA Connectors |
| PWR_S4P_H CN4 | SATA POWER |
| PWR_S4P_H CN6 | SATA POWER |
| LAN1 | INTEL I217-LM |
| LAN2 | INTEL I210-IT |
| F_USB1 | USB2.0 |
| CN18 | USB3.0 X2 |
| CN19 | USB3.0 X2 |
| MIC 1 | Audio Jacks Connector |
| LOUT1 | Audio Jacks Connector |
| DIO1 | Digital I/O Box Head |
| SW2 | POWER On/Off Switch |
| PWRIN1 | DC Adapter Power Input |
| CN11 | UPDATE BIOS |
| DP1 | DISPLAY PORT |
| DP2 | DISPLAY PORT |
| DVI | DVI-I |
| SIM_CARD_1 | SIM card socket |
| JP7 | COM3 +12/+5V selection |
| JP14 | COM4 +12/+5V selection |
| JP15 | COM5 +12/+5V selection |
| JP16 | COM6 +12/+5V selection |
| COM1 | RS232/422/485 with 5V/12V selectable |
| COM2 | RS232/422/485 with 5V/12V selectable |
| COM3 | RS232 with 5V/12V selectable |
| COM4 | RS232 with 5V/12V selectable |
| COM5 | RS232 with 5V/12V selectable |

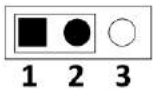
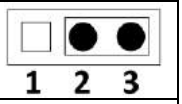
| | |
|---|---|
| COM6 | RS232 with 5V/12V selectable |
| DC JACK | DC connector |
| CON A1 | CONNECTOR A TOP |
| CPU FAN | CPU FAN CONNECTOR |
| SYSFAN1 | SYSTEM FAN CONNECTOR |
| JP19 | LVDS Display |
| JV8, JV9, JV10, JV11 | LVDS Panel selection jumper setting |
| JV12 | LVDS_VDD power select |
| JP17, JP18 | LVDS Backlight Brightness Control |
| LAN_SEL3 | StackPC/I217-LM selection |
| LAN_SEL2 | StackPC/I210-IT selection |
| MCARD_SEL1 | mSATA and mPCIE selection |
| JV2, JV3 | COM1 RS232/422/485 jumper setting |
| JV4 | COM1 RS422/485 receiver termination |
| JP12 | COM1P9SEL pin function select |
| JV7, JV6 | COM2 RS232/422/485 jumper setting |
| JV5 | COM2 RS422/485 receiver termination |
| JP13 | COM2 5V/12V selection |
| FPE1 | StackPC FPE Top Connector |
| LED1 | LAN1 LED STATUS |
| LED2 | LAN2 LED STATUS |
| LED3 | POWER/HDD LED |
| SW1 | POWER BUTTON |
| FPR5 | RESET POWER BUTTON |
| JBKL1 | LVDA POWER BOX HEADER |
| FP1 | Front Panel |
| FP3 | LAN LED |
| JPEG1, JPEG2 | Clear CMOS |
| JPEG4 | Flash Descriptor Security Overide |
| J3 | Touch Connector |
| JP22 | PEG DEFER TRAINING |
| JP20, JP21 | PCI Express Bifurcation |

## 2.2 Jumper Setting

**JV2,3: COM1 RS232/422/485 jumper setting**

| No. | Function Description | JV3 | JV2 | Location |
|---|---|---|---|---|
| 1 | Loopback |   |   |   |
| 2 | RS232 (Default) |   |   | |
| 3 | RS485 Half-Duplex |   |   | |
| 4 | RS485/422 Full Duplex |   |   | |

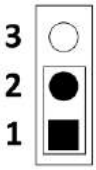
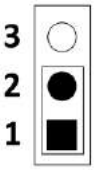
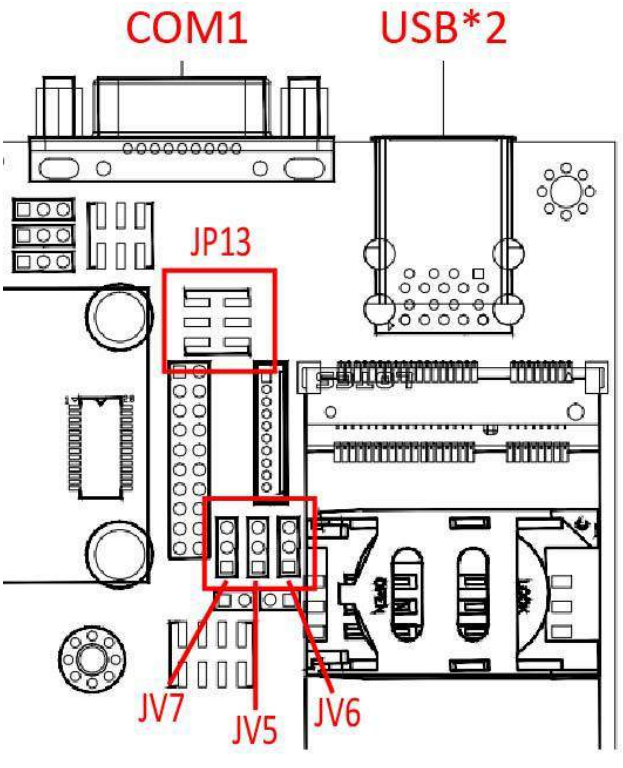
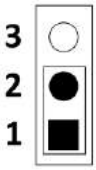
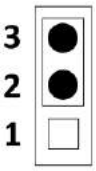
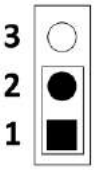
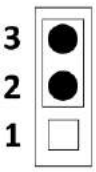
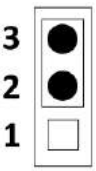
**JV4: COM1 RS422/485 receiver termination**

| Jumper | Function description | Setting |
|---|---|---|
| 1-2 | Disable RS422/485 receiver termination (default) |   |
| 2-3 | Enable RS422/485receiver termination |   |
| Default setting: 1-2 | | |

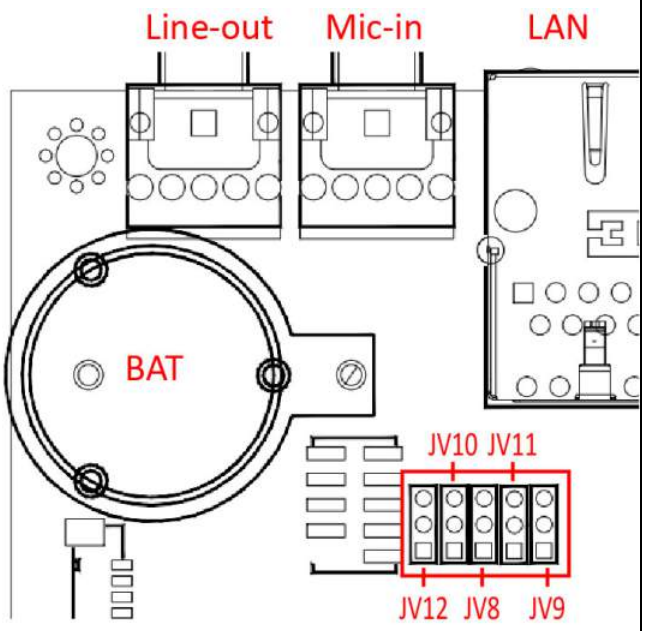
**JV5: COM2 RS422/485 receiver termination**

| Jumper | Function description | Setting |
|---|---|---|
| 1-2 | Disable RS422/485 receiver termination (default) |   |
| 2-3 | Enable RS422/485 receiver termination |   |

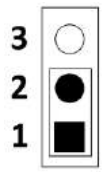
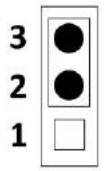
**JV6,7: COM2 RS232/422/485 jumper setting**

| No. | Function Description | JV6 | JV7 | Location |
|---|---|---|---|---|
| 1 | Loopback |   |   |   |
| 2 | RS232 (Default) |   |   | |
| 3 | RS485 Half-Duplex |   |   | |
| 4 | RS485/422 Full-Duplex |   |   | |

**JV8,9,10,11: LVDS Panel selection jumper setting**

| No. | HA (Pixel) | VA (Line) | Color depth | JV10 | JV8 | JV11 | JV9 | Location |
|---|---|---|---|---|---|---|---|---|
| **1.** | 800 | 600 | 18-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 |  |
| 2 | 1024 | 768 | 24-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 | |
| 3 | 1024 | 768 | 18-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 | |
| 4 | 1280 | 800 | 18-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 | |
| 5 | 1280 | 1024 | 24-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 | |
| 6 | 1366 | 768 | 24-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 | |
| 7 | 1440 | 900 | 24-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 | |
| 8 | 1920 | 1080 | 24-bit | 3 2 1 | 3 2 1 | 3 2 1 | 3 2 1 | |

**JV12: LVDS_VDD power select**

| Jumper | Function description | Setting |
|---|---|---|
| 1-2 | 3.3V |   |
| 2-3 | 5.0V |   |
| Default setting: 1-2 | | |

**JP12: COM1P9SEL pin function select**

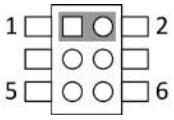
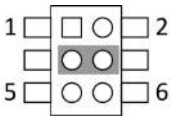
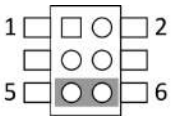
**JP13: COM2P9SEL pin function select**

**JP7: COM3P9SEL pin function select**

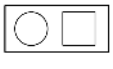
**JP14: COM4P9SEL pin function select**

**JP15: COM5P9SEL pin function select**

**JP16: COM6P9SEL pin function select**

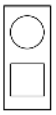
| Jumper | Function description | Setting |
|---|---|---|
| 1-2 | COM_RI |   |
| 3-4 | 5VS |   |
| 5-6 | 12V |   |

**JP17, JP18: LVDS Backlight Brightness Control**

| Jump | PIN | Definition | Setting | Function | |
|---|---|---|---|---|---|
| JP17 | 1 | BLUP | Short (1-2) | short once, increase brightness one step |  |
| | 2 | GND | | | |
| JP18 | 1 | BLDN | Short (1-2) | short once, decrease brightness one step |  |
| | 2 | GND | | | |
| Take cable to each two push-button for user<br>Default: Open (1-2) | | | | | |

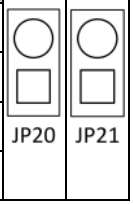
**JP19: LVDS Display**

| PIN | Definition | Jump setting | Function |
|---|---|---|---|
| 1 | CFG4 | Short (1-2) | Enable |
| 2 | GND | Open (1-2) (Default) | Disable |



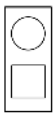
**JP20, JP21: PCI Express Bifurcation**

| JP20 | JP21 | Function |
|---|---|---|
| short | short | 1 x8, 2 x4 PCI Express |
| open | short | Reserved |
| short | open | 2 x8 PCI Express (SK210) |
| open | open | 1 x16 PCI Express (Default) |




**JP22: PEG DEFER TRAINING**

| PIN | Definition | Setting | Function |
|---|---|---|---|
| 1 | CFG7 | Short (1-2) | PEG Wait for BIOS for training |
| 2 | GND | Open (1-2) (Default) | PEG Train immediately Following xxRESETB de assertion |



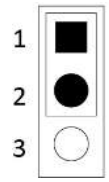
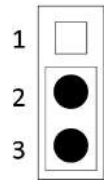
**JPEG1, JPEG2: Clear CMOS**

| Jump | Function | |
|---|---|---|
| JPEG1 | short 3second to clear ME |  |
| JPEG2 | short 3second to clear BIOS |  |
| Must short JEPG1 first. | | |

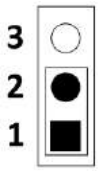
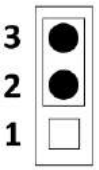
**JPEG4: Flash Descriptor Security Overide**

| PIN | Jump setting | Function | |
|---|---|---|---|
| 1 | Short (1-2) | Enable |  |
| 2 | Open (1-2) (Default) | Disable | |

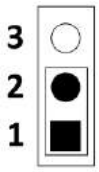
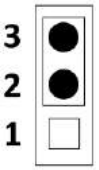
**MCARD_SEL1: mSATA and mPCIE selection**

| Jumper | Function description | Setting |
|---|---|---|
| 1-2 | mPCIE |   |
| 2-3 | mSATA (Default) |   |

**LAN_SEL3: StackPC/I217-LM selection**

| Jumper | Function description | Setting |
|---|---|---|
| 1-2 | STACK PC |   |
| 2-3 | I217-LM (Default) |   |

**LAN_SEL2: StackPC/I210-IT selection**

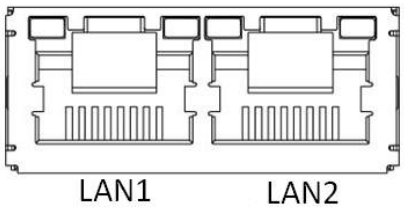
| Jumper | Function description | Setting |
|---|---|---|
| 1-2 | STACK PC |   |
| 2-3 | I210-IT (Default) |   |

### 2.3 Connector

**LAN1: Intel I217-LM**

**LAN2: Intel I210-IT**

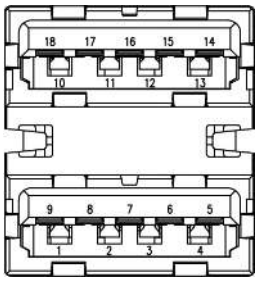
| LAN1 | | LAN2 | |
|---|---|---|---|
| PIN | DEFINITION | PIN | DEFINITION |
| A1 | LAN1_MDI0_DP | B1 | LAN2_MDIP0 |
| A2 | LAN1_MDI0_DN | B2 | LAN2_MDIN0 |
| A3 | LAN1_MDI1_DP | B3 | LAN2_MDIP1 |
| A4 | LAN1_MDI1_DN | B4 | LAN2_MDIN1 |
| A7 | LAN1_MDI2_DP | B7 | LAN2_MDIP2 |
| A8 | LAN1_MDI2_DN | B8 | LAN2_MDIN2 |
| A9 | LAN1_MDI3_DP | B9 | LAN2_MDIP3 |
| A10 | LAN1_MDI3_DN | B10 | LAN2_MDIN3 |




**USB3.0 CN18: USB3.0*2**

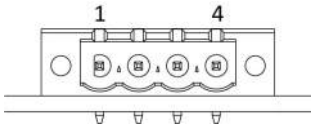
**USB3.0 CN19: USB3.0*2**

| LOWER USB | | UPPER USB | |
|---|---|---|---|
| PIN | DEFINITION | PIN | DEFINITION |
| 1 | USB_VCC | 10 | USB_VCC |
| 2 | USBD- | 11 | USBD- |
| 3 | USBD+ | 12 | USBD+ |
| 4 | GND | 13 | GND |
| 5 | USB_SSRXN_C | 14 | USB_SSRXN_C |
| 6 | USB_SSRXP_C | 15 | USB_SSRXP_C |
| 7 | GND | 16 | GND |
| 8 | USB3TN | 17 | USB3TN |
| 9 | USB3TP3 | 18 | USB3TP4 |



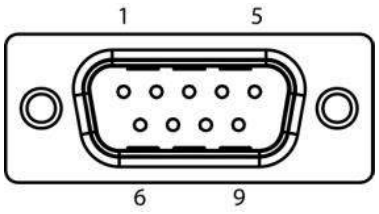

**PWRIN1: DC Adapter Power Input**

| PIN | DEFINITION |
|---|---|
| 1 | +VIN |
| 2 | +VIN |
| 3 | GND |
| 4 | GND |



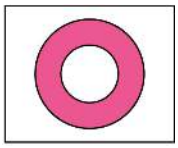
**COM1: RS232/422/485 with 5V/12V selectable**

| Pin | RS-232 | RS-422 | Half Duplex RS-485 |
|---|---|---|---|
| 1 | DCD# | TX- | D- |
| 2 | RXD | TX+ | D+ |
| 3 | TXD | RX+ | NA |
| 4 | DTR# | RX- | NA |
| 5 | GND | GND | GND |
| 6 | DSR# | NA | NA |
| 7 | RTS# | NA | NA |
| 8 | CTS# | NA | NA |
| 9 | RI# (Define by JP12) | RI# (Define by JP12) | RI# (Define by JP12) |



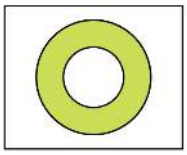

**MIC 1: Audio Jacks Connector**

| PIN | DEFINITION |
|---|---|
| 5 | MIC_L |
| 4 | GND |
| 3 | NC |
| 2 | MIC1_R |
| 1 | GND |



**LOUT 1: Audio Jacks Connector**

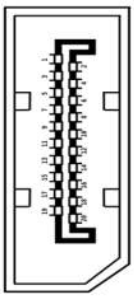
| PIN | DEFINITION |
|---|---|
| 5 | FRONT_L |
| 4 | GND |
| 3 | NC |
| 2 | FRONT_R |
| 1 | GND |



**DP1: DISPLAY PORT**

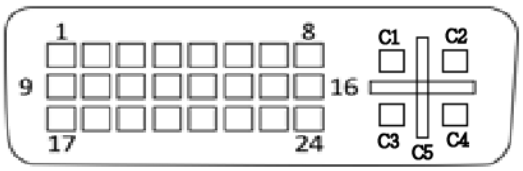
**DP2: DISPLAY PORT**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | DPC_LANEP0 | 2 | GND |
| 3 | DPC_LANEN0 | 4 | DPC_LANEP1 |
| 5 | GND | 6 | DPC_LANEN1 |
| 7 | DPC_LANEP2 | 8 | GND |
| 9 | DPC_LANEN2 | 10 | DPC_LANEP3 |
| 11 | GND | 12 | DPC_LANEN3 |
| 13 | DDIC_DDC_AUX_SEL | 14 | GND |
| 15 | DPC_AUXP | 16 | GND |
| 17 | DPC_AUXN | 18 | DPC_DET |
| 19 | GND | 20 | DPC_PWR |



**DVI: DVI-I**

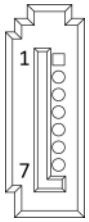
| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | TMDS Data2- | 13 | NC |
| 2 | TMDS Data2+ | 14 | +5V Power |
| 3 | GND | 15 | GND |
| 4 | NC | 16 | Hot Plug Detect |
| 5 | NC | 17 | TMDS Data0- |
| 6 | DDC Clock | 18 | TMDS Data0+ |
| 7 | DDC Data | 19 | GND |
| 8 | Analog VSYNC | 20 | NC |
| 9 | TMDS Data1- | 21 | NC |
| 10 | TMDS Data1+ | 22 | GND |
| 11 | GND | 23 | TMDS Clock+ |
| 12 | NC | 24 | TMDS Clock- |
| C1 | Analog Red | C2 | Analog Green |
| C3 | Analog Blue | C4 | Analog HYNC |
| C5 | Analog GND0 | C6 | Analog GND1 |



**SATA-CON CN3: Serial ATA Connectors**

**SATA-CON CN5: Serial ATA Connectors**

| PIN | DEFINITION |
|---|---|
| 1 | GND |
| 2 | TXP |
| 3 | TXN |
| 4 | GND |
| 5 | RXN |
| 6 | RXP |
| 7 | GND |



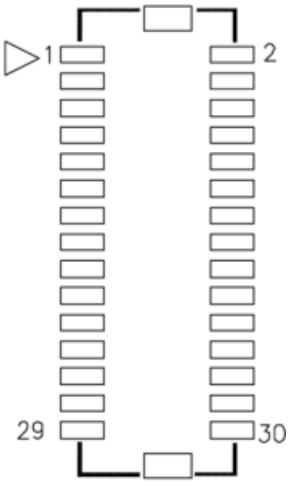

**PWR_S4P_H CN4: SATA POWER**

**PWR_S4P_H CN6: SATA POWER**

| PIN | DEFINITION |
|---|---|
| 1 | 12V |
| 2 | GND |
| 3 | GND |
| 4 | 5VS |

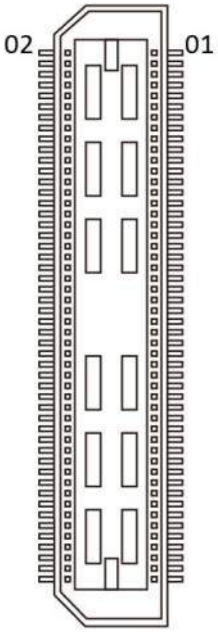

**LVDS1: LVDS CONNECTOR**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | LVDS_BCLK | 2 | GND |
| 3 | LVDS_BCLK# | 4 | LVDS_A3 |
| 5 | GND | 6 | LVDS_A3# |
| 7 | LVDS_B3 | 8 | GND |
| 9 | LVDS_B3# | 10 | LVDS_ACLK |
| 11 | LVDS_B2 | 12 | LVDS_ ACLK # |
| 13 | LVDS_B2# | 14 | GND |
| 15 | LVDS_B1 | 16 | LVDS_A2 |
| 17 | LVDS_B1# | 18 | LVDS_A2# |
| 19 | LVDS_B0 | 20 | LVDS_A1 |
| 21 | LVDS_B0# | 22 | LVDS_A1# |
| 23 | GND | 24 | LVDS_A0 |
| 25 | LVDS_DCC_SC | 26 | LVDS_A0# |
| 27 | LVDS_DCC_SD | 28 | GND |
| 29 | LVDS_VDD (define by JV12) | 30 | LVDS_VDD (define by JV12) |



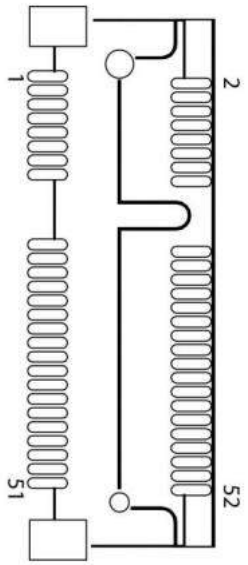
**DIMMA1: DDR3 SO DIMM Socket**

| PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VSS | 41 | DQ16 | 81 | VSS | 121 | CK1 | 161 | DQS4# | 201 | VSS |
| 2 | VSS | 42 | VSS | 82 | DM8 | 122 | A1 | 162 | VSS | 202 | DQ55 |
| 3 | VSS | 43 | DQ17 | 83 | DQS8# | 123 | CK1# | 163 | DQS4 | 203 | DQ50 |
| 4 | VSS | 44 | VREFDQ | 84 | VSS | 124 | VDD | 164 | DM4 | 204 | VSS |
| 5 | DQ0 | 45 | VSS | 85 | DQS8 | 125 | VDD | 165 | VSS | 205 | DQ51 |
| 6 | DQ4 | 46 | NC(TEST) | 86 | CB6 | 126 | CK0 | 166 | VSS | 206 | DQ60 |
| 7 | DQ1 | 47 | DQS2# | 87 | VSS | 127 | VREFCA | 167 | DQ34 | 207 | VSS |
| 8 | DQ5 | 48 | VSS | 88 | CB7 | 128 | CK0# | 168 | DQ38 | 208 | DQ61 |
| 9 | VSS | 49 | DQS2 | 89 | CB2 | 129 | PAR_IN | 169 | DQ35 | 209 | DQ56 |
| 10 | VSS | 50 | DM2 | 90 | VSS | 130 | VDD | 170 | DQ39 | 210 | VSS |
| 11 | DQS0# | 51 | VSS | 91 | CB3 | 131 | VDD | 171 | VSS | 211 | DQ57 |
| 12 | DM0 | 52 | VSS | 92 | RESET# | 132 | EVENT# | 172 | VSS | 212 | DM7 |
| 13 | DQS0 | 53 | DQ18 | 93 | VSS | 133 | A10 | 173 | DQ40 | 213 | VSS |
| 14 | VSS | 54 | DQ22 | 94 | ERR_OUT# | 134 | A0 | 174 | DQ44 | 214 | VSS |
| 15 | VSS | 55 | DQ19 | 95 | VTT | 135 | BA0 | 175 | DQ41 | 215 | DQS7# |
| 16 | DQ6 | 56 | DQ23 | 96 | VTT | 136 | VDD | 176 | DQ45 | 216 | DQ62 |
| 17 | DQ2 | 57 | VSS | 97 | CKE0 | 137 | VDD | 177 | VSS | 217 | DQS7 |
| 18 | DQ7 | 58 | VSS | 98 | CKE1 | 138 | BA1 | 178 | VSS | 218 | DQ63 |
| 19 | DQ3 | 59 | DQ24 | 99 | VDD | 139 | WE# | 179 | DQS5# | 219 | VSS |
| 20 | VSS | 60 | DQ28 | 100 | VDD | 140 | VDD | 180 | DM5 | 220 | VSS |
| 21 | VSS | 61 | DQ25 | 101 | BA2 | 141 | CAS# | 181 | DQS5 | 221 | DQ58 |
| 22 | DQ12 | 62 | DQ29 | 102 | A15 | 142 | RAS# | 182 | VSS | 222 | VDD_SPD |
| 23 | DQ8 | 63 | VSS | 103 | VDD | 143 | VDD | 183 | VSS | 223 | DQ59 |
| 24 | DQ13 | 64 | VSS | 104 | A14 | 144 | S0# | 184 | DQ46 | 224 | SA0 |
| 25 | DQ9 | 65 | DQS3# | 105 | A11 | 145 | S1# | 185 | DQ42 | 225 | VSS |
| 26 | VSS | 66 | DM3 | 106 | VDD | 146 | VDD | 186 | DQ47 | 226 | SA1 |
| 27 | VSS | 67 | DQS3 | 107 | A7 | 147 | ODT1 | 187 | DQ43 | 227 | SA2 |
| 28 | DM1 | 68 | VSS | 108 | A12 | 148 | ODT0 | 188 | VSS | 228 | SCL |
| 29 | DQS1# | 69 | VSS | 109 | VDD | 149 | VDD | 189 | VSS | 229 | VSS |
| 30 | VSS | 70 | DQ30 | 110 | A9 | 150 | A13 | 190 | DQ52 | 230 | SDA |
| 31 | DQS1 | 71 | DQ26 | 111 | A5 | 151 | S3# | 191 | DQ48 | 231 | SATA_TX0 |
| 32 | DQ14 | 72 | DQ31 | 112 | VDD | 152 | VDD | 192 | DQ53 | 232 | VSS |
| 33 | VSS | 73 | DQ27 | 113 | A4 | 153 | VSS | 193 | DQ49 | 233 | SATA_TX0# |
| 34 | DQ15 | 74 | VSS | 114 | A8 | 154 | S2# | 194 | VSS | 234 | SATA_TX1# |
| 35 | DQ10 | 75 | VSS | 115 | VDD | 155 | DQ32 | 195 | VSS | 235 | VSS |
| 36 | VSS | 76 | CB4 | 116 | A6 | 156 | VSS | 196 | DM6 | 236 | SATA_TX1 |
| 37 | DQ11 | 77 | CB0 | 117 | A2 | 157 | DQ33 | 197 | DQS6# | 237 | VTT |
| 38 | DQ20 | 78 | CB5 | 118 | VDD | 158 | DQ36 | 198 | VSS | 238 | VSS |
| 39 | VSS | 79 | CB1 | 119 | VDD | 159 | VSS | 199 | DQS6 | 239 | VTT |
| 40 | DQ21 | 80 | VSS | 120 | A3 | 160 | DQ37 | 200 | DQ54 | 240 | VTT |



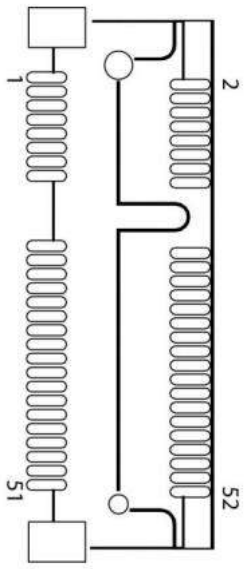
**MCARD1: Mini PCIE Card Slot<COLAY M SATA>**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | WAKE# | 2 | 3.3VAUX |
| 3 | COEX1 | 4 | GND |
| 5 | COEX2 | 6 | 1.5V |
| 7 | CLKREQ# | 8 | UIM_PWR |
| 9 | GND | 10 | UIM_DATA |
| 11 | REFCLK- | 12 | UIM_CLK |
| 13 | REFCLK+ | 14 | UIM_RESET |
| 15 | GND | 16 | UIM_VPP |
| 17 | Reserved | 18 | GND |
| 19 | Reserved | 20 | W_Disable# |
| 21 | GND | 22 | PERST# |
| 23 | PERn0 | 24 | +3.3Vaux |
| 25 | PERp0 | 26 | GND |
| 27 | GND | 28 | 1.5V |
| 29 | GND | 30 | SMB_CLK |
| 31 | PETn0 | 32 | SMB_DATA |
| 33 | PETp0 | 34 | GND |
| 35 | GND | 36 | USB_D- |
| 37 | GND | 38 | USB_D+ |
| 39 | +3.3VAUX | 40 | GND |
| 41 | +3.3VAUX | 42 | LED_WWAN# |
| 43 | GND | 44 | LED_WLAN# |
| 45 | Reserved | 46 | LED_WPAN# |
| 47 | Reserved | 48 | 1.5V |
| 49 | Reserved | 50 | GND |
| 51 | Reserved | 52 | 3.3VAUX |



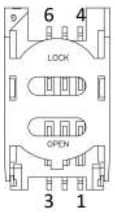
**MINI MPCIE: Mini PCIE Card Slot**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | WAKE# | 2 | 3.3V |
| 3 | Reserved | 4 | GND |
| 5 | Reserved | 6 | 1.5V |
| 7 | CLKREQ# | 8 | UIM_PWR |
| 9 | GND | 10 | UIM_DATA |
| 11 | REFCLK- | 12 | UIM_CLK |
| 13 | REFCLK+ | 14 | UIM_RESET |
| 15 | GND | 16 | UIM_VPP |
| 17 | Reserved | 18 | GND |
| 19 | Reserved | 20 | W_Disable# |
| 21 | GND | 22 | PERST# |
| 23 | PERn0 | 24 | 3.3Vaux |
| 25 | PERp0 | 26 | GND |
| 27 | GND | 28 | 1.5V |
| 29 | GND | 30 | SMB_CLK |
| 31 | PETn0 | 32 | SMB_DATA |
| 33 | PETp0 | 34 | GND |
| 35 | GND | 36 | USB_D- |
| 37 | Reserved | 38 | USB_D+ |
| 39 | Reserved | 40 | GND |
| 41 | Reserved | 42 | LED_WWAN# |
| 43 | Reserved | 44 | LED_WLAN# |
| 45 | Reserved | 46 | LED_WPAN# |
| 47 | Reserved | 48 | 1.5V |
| 49 | Reserved | 50 | GND |
| 51 | Reserved | 52 | 3.3V |



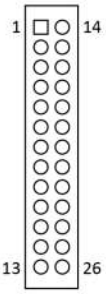

**SIM_CARD1: SIM card socket**

| PIN | DEFINITION |
|---|---|
| 1 | VCC |
| 2 | RESET |
| 3 | CLOCK |
| 4 | GND |
| 5 | VPP |
| 6 | DATA |



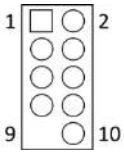
**DIO1: Digital I/O Box Head**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | DIO0 | 2 | DIO1 |
| 3 | DIO2 | 4 | DIO3 |
| 5 | DIO4 | 6 | DIO5 |
| 7 | DIO6 | 8 | DIO7 |
| 9 | DIO8 | 10 | DIO9 |
| 11 | DIO10 | 12 | DIO11 |
| 13 | DIO12 | 14 | DIO13 |
| 15 | DIO14 | 16 | DIO15 |
| 17 | 5VS | 18 | GND |
| 19 | 5VS | 20 | GND |




**F_USB1: USB**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | USBV4 | 2 | USBV5 |
| 3 | USBD4- | 4 | USBD5- |
| 5 | USBD4+ | 6 | USBD5+ |
| 7 | GND | 8 | GND |
| 9 | NC | 10 | GND |




**COM2: RS232/422/485 with 5V/12V selectable**

| PIN | DEFINITION |
|---|---|
| 1 | 5VS |
| 2 | GND |
| 3 | COM2P9SEL |
| 4 | DTR2#_OPTO |
| 5 | CTS2#_OPTO |
| 6 | TXD2_OPTO |
| 7 | RTS2#_OPTO |
| 8 | RXD2_OPTO |
| 9 | DSR2#_OPTO |
| 10 | DCD2#_OPTO |

**COM3: RS232 with 5V/12V selectable**

**COM4: RS232 with 5V/12V selectable**

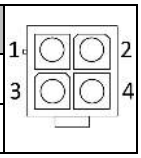
**COM5: RS232 with 5V/12V selectable**

**COM6: RS232 with 5V/12V selectable**

| PIN | DEFINITION |
|---|---|
| 1 | 5VS |
| 2 | GND |
| 3 | COM3P9SEL |
| 4 | COM3_DTR- |
| 5 | COM3_CTS- |
| 6 | COM3_TXD |
| 7 | COM3_RTS- |
| 8 | COM3_RXD |
| 9 | COM3_DSR- |
| 10 | COM3_DCD- |

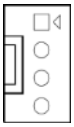

**DC Jack**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | GND | 2 | GND |
| 3 | +VIN | 4 | +VIN |



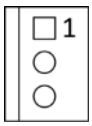

**CPU FAN: CPU FAN CONNECTOR**

| PIN | DEFINITION |
|---|---|
| 1 | CPUFAN_PWN |
| 2 | CPUFAN_IO |
| 3 | CPUFAN_VCC |
| 4 | GND |



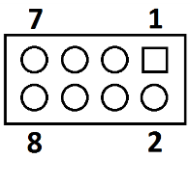
**SYSFAN1: SYSTEM FAN CONNECTOR**

| PIN | DEFINITION |
|---|---|
| 1 | SYSFANIO |
| 2 | SYSFAN_VCC |
| 3 | GND |



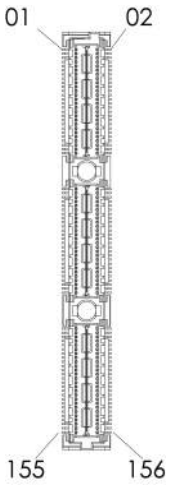

**CN11: Update BIOS**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | SPI_CE0#_F | 2 | VCC |
| 3 | SPI_SI_F | 4 | -SPI_HOLD |
| 5 | SPI_WP# | 6 | SPI_CLK_F |
| 7 | GND | 8 | SPI_SO_F |



**CON A1: CONNECTOR A TOP**

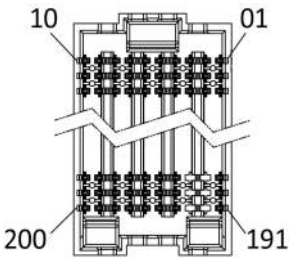
| PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | USB_OC#6 | 2 | BUF_PLT_RST- | 53 | 3V3_DU | 54 | 3V3_DU | 105 | GND | 106 | CLK_LPC_UART |
| 3 | 3.3V | 4 | 3.3V | 55 | 3V3_DU | 56 | GND | 107 | NC | 108 | GND |
| 5 | USBD7+ | 6 | USBD6+ | 57 | ST_LAN1_MDIP0 | 58 | NC | 109 | ST_LAN1_MDIP2 | 110 | |
| 7 | USBD7- | 8 | USBD6- | 59 | ST_LAN1_MDIN0 | 60 | NC | 111 | ST_LAN1_MDIN2 | 112 | |
| 9 | GND | 10 | GND | 61 | GND | 62 | GND | 113 | GND | 114 | GND |
| 11 | PCIE_TXP5 | 12 | PCIE_TXP7 | 63 | ST_LAN2_MDIP0 | 64 | NC | 115 | ST_LAN2_MDIP2 | 116 | |
| 13 | PCIE_TXN5 | 14 | PCIE_TXN7 | 65 | ST_LAN2_MDIN0 | 66 | NC | 117 | ST_LAN2_MDIN2 | 118 | |
| 15 | GND | 16 | GND | 67 | GND | 68 | GND | 119 | GND | 120 | GND |
| 17 | PCIE_TXP6 | 18 | PCIE_TXP8 | 69 | ST_LAN1_MDIP1 | 70 | NC | 121 | ST_LAN1_MDIP3 | 122 | |
| 19 | PCIE_TXN6 | 20 | PCIE_TXN8 | 71 | ST_LAN1_MDIN1 | 72 | NC | 123 | ST_LAN1_MDIN3 | 124 | |
| 21 | GND | 22 | GND | 73 | GND | 74 | GND | 125 | GND | 126 | GND |
| 23 | PCIE_RXP5 | 24 | PCIE_RXP7 | 75 | ST_LAN2_MDIP1 | 76 | NC | 127 | ST_LAN2_MDIP3 | 128 | ST_LAN2_MDIP3 |
| 25 | PCIE_RXN5 | 26 | PCIE_RXN7 | 77 | ST_LAN2_MDIN1 | 78 | NC | 129 | ST_LAN2_MDIN3 | 130 | ST_LAN2_MDIN3 |
| 27 | GND | 28 | GND | 79 | ST_LAN2_ACT# | 80 | ST_LAN1_ACT# | 131 | PE_PRSNT1_A- | 132 | PE_PRSNT0_A |
| 29 | PCIE_RXP6 | 30 | PCIE_RXP8 | 81 | SATATXP5 | 82 | SATATXP4 | 133 | SATSRXP5 | 134 | SATARXP5 |
| 31 | PCIE_RXN6 | 32 | PCIE_RXN8 | 83 | SATATXN5 | 84 | SATATXN4 | 135 | SATSRXN5 | 136 | SATARXN5 |
| 33 | GND | 34 | GND | 85 | GND | 86 | GND | 137 | GND | 138 | GND |
| 35 | PEX5_PCIE_CLK | 36 | PEX7_PCIE_CLK | 87 | USBD9+ | 88 | USBD11+ | 139 | NC | 140 | |
| 37 | PEX5_PCIE_CLK# | 38 | PEX7_PCIE_CLK# | 89 | USBD9- | 90 | USBD11- | 141 | NC | 142 | |
| 39 | 5V_DU | 40 | 5V_DU | 91 | GND | 92 | GND | 143 | GND | 144 | GND |
| 41 | PEX6_PCIE_CLK | 42 | PEX8_PCIE_CLK | 93 | NC | 94 | USBD10+ | 145 | LPC_AD0 | 146 | LPC_LDRO0 |
| 43 | PEX6_PCIE_CLK# | 44 | PEX8_PCIE_CLK# | 95 | NC | 96 | USBD10- | 147 | LPC_AD1 | 148 | INT_SERIRQ |
| 45 | GND | 46 | 5VS | 97 | GND | 98 | GND | 149 | GND | 150 | GND |
| 47 | SMB_DATA_MAIN | 48 | NC | 99 | ETH_1_CTREF | 100 | ETH_0_CTREF | 151 | LPC_AD2 | 152 | LPC_FRAME |
| 49 | SMB_CLK_MAIN | 50 | NC | 101 | SPI_MISO_AA | 102 | SPI_CE0#_F | 153 | LPC_AD3 | 154 | VRTC |
| 51 | SMBALERT# | 52 | BUS_PS_ON# | 103 | SPI_SI_F | 104 | SPI_CE1#_F | 155 | FUSB_1RTS- | 156 | FUSB_ORTS |



**FPE1: StackPC FPE Top Connector**

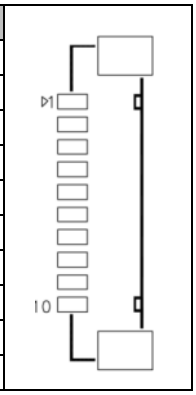
| PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|---|---|---|---|---|---|
| 1 | NC | 2 | NC | 3 | NC | 4 | NC | 5 | NC |
| 11 | GND | 12 | NC | 13 | GND | 14 | NC | 15 | GND |
| 21 | NC | 22 | NC | 23 | NC | 24 | GND | 25 | NC |
| 31 | NC | 32 | NC | 33 | NC | 34 | NC | 35 | NC |
| 41 | GND | 42 | NC | 43 | GND | 44 | NC | 45 | GND |
| 51 | NC | 52 | GND | 53 | NC | 54 | GND | 55 | NC |
| 61 | NC | 62 | NC | 63 | NC | 64 | NC | 65 | NC |
| 71 | GND | 72 | NC | 73 | GND | 74 | NC | 75 | GND |
| 81 | PEG_TXP0 | 82 | NC | 83 | PEG_TXP2 | 84 | GND | 85 | PEG_TXP4 |
| 91 | PEG_TXN0 | 92 | PEG_TXP1 | 93 | PEG_TXN2 | 94 | PEG_TXP3 | 95 | PEG_TXN4 |
| 101 | GND | 102 | PEG_TXN1 | 103 | GND | 104 | PEG_TXN3 | 105 | GND |
| 111 | PEG_RXP_0 | 112 | GND | 113 | PEG_RXP_2 | 114 | GND | 115 | PEG_RXP_4 |
| 121 | PEG_RXN_0 | 122 | PEG_RXP_1 | 123 | PEG_RXN_2 | 124 | PEG_RXP_3 | 125 | PEG_RXN_4 |
| 131 | GND | 132 | PEG_RXN_1 | 133 | GND | 134 | PEG_RXN_3 | 135 | GND |
| 141 | PEG_TXP8 | 142 | GND | 143 | PEG_TXP10 | 144 | GND | 145 | PEG_TXP12 |
| 151 | PEG_TXN8 | 152 | PEG_TXP9 | 153 | PEG_TXN10 | 154 | PEG_TXP11 | 155 | PEG_TXN12 |
| 161 | GND | 162 | PEG_TXN9 | 163 | GND | 164 | PEG_TXN11 | 165 | GND |
| 171 | PEG_RXP_8 | 172 | GND | 173 | PEG_RXP_10 | 174 | GND | 175 | PEG_RXP_12 |
| 181 | PEG_RXN_8 | 182 | PEG_RXP_9 | 183 | PEG_RXN_10 | 184 | PEG_RXP_11 | 185 | PEG_RXN_12 |
| 191 | GND | 192 | PEG_RXN_9 | 193 | GND | 194 | PEG_RXN_11 | 195 | GND |

| PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME |
|---|---|---|---|---|---|---|---|---|---|
| 6 | NC | 7 | NC | 8 | NC | 9 | NC | 10 | NC |
| 16 | NC | 17 | GND | 18 | NC | 19 | NC | 20 | NC |
| 26 | GND | 27 | NC | 28 | GND | 29 | NC | 30 | NC |
| 36 | NC | 37 | NC | 38 | NC | 39 | NC | 40 | NC |
| 46 | NC | 47 | GND | 48 | NC | 49 | GND | 50 | NC |
| 56 | GND | 57 | NC | 58 | GND | 59 | NC | 60 | NC |
| 66 | NC | 67 | NC | 68 | NC | 69 | SPKR | 70 | NC |
| 76 | NC | 77 | GND | 78 | NC | 79 | GND | 80 | NC |
| 86 | GND | 87 | PEG_TXP6 | 88 | GND | 89 | NC | 90 | CFG5 |
| 96 | PEG_TXP5 | 97 | PEG_TXN6 | 98 | PEG_TXP7 | 99 | NC | 100 | CFG6 |
| 106 | PEG_TXN5 | 107 | GND | 108 | PEG_TXN7 | 109 | GND | 110 | BUF_PLT_RST- |
| 116 | GND | 117 | PEG_RXP_6 | 118 | GND | 119 | PEG_A_CLK_P | 120 | GND |
| 126 | PEG_RXP_5 | 127 | PEG_RXN_6 | 128 | PEG_RXP_7 | 129 | PEG_A_CLK_N | 130 | 3V3_DU |
| 136 | PEG_RXN_5 | 137 | GND | 138 | PEG_RXN_7 | 139 | GND | 140 | 3V3_DU |
| 146 | GND | 147 | PEG_TXP14 | 148 | GND | 149 | PEG_B_CLK_P | 150 | GND |
| 156 | PEG_TXP13 | 157 | PEG_TXN14 | 158 | PEG_TXP15 | 159 | PEG_B_CLK_N | 160 | GND |
| 166 | PEG_TXN13 | 167 | GND | 168 | PEG_TXN15 | 169 | GND | 170 | NC |
| 176 | GND | 177 | PEG_RXP_14 | 178 | GND | 179 | NC | 180 | 12V |
| 186 | PEG_RXP_13 | 187 | PEG_RXN_14 | 188 | PEG_RXP_15 | 189 | NC | 190 | 12V |
| 196 | PEG_RXN_13 | 197 | GND | 198 | PEG_RXN_15 | 199 | NC | 200 | 12V |



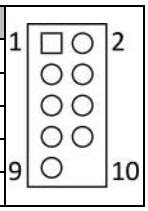
**JBKL1: JBKL1: Inverter connector**

| PIN | DEFINITION |
|---|---|
| 1 | 12V |
| 2 | 12V |
| 3 | 12V |
| 4 | 5VS |
| 5 | 5VS |
| 6 | GND |
| 7 | GND |
| 8 | BL_EN |
| 9 | LVDS0_BKL_CTRL_R |
| 10 | GND |



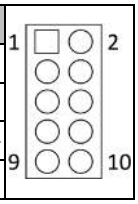

**FP1: Front Panel**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | HDLED+ | 2 | PLED+ |
| 3 | HDLED- | 4 | GND |
| 5 | GND | 6 | EC_PWR_BTN |
| 7 | EXT_RESET# | 8 | GND |
| 9 | NC | 10 | NC |




**FP3: LAN LED**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | 3V3M | 2 | 3V3M |
| 3 | LAN_LED_LNK#_ACT | 4 | LAN2_ACT# |
| 5 | LAN_LED_LNK_1000# | 6 | LAN2_LED_1000- |
| 7 | LAN_LED_LNK_100# | 8 | LAN2_LED_100- |




**Plug LED cable to FP3 pin header**

Active LED: plug 1-3 pin

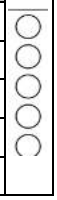
Single 1000M LED: plug 1-5 pin

Single 100M LED: plug 1-7 pin

Dual 1000M LED: plug 5-7 pin

**J3: Touch Connector**

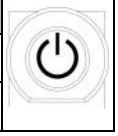
| PIN | DEFINITION |
|---|---|
| 1 | X+ |
| 2 | Y+ |
| 3 | X- |
| 4 | Y- |
| 5 | Sense |



**2.4 Switch**

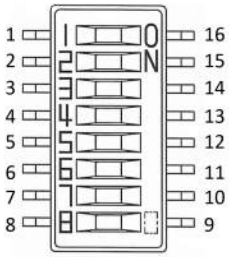
**SW1: POWER BUTTON**

| PIN | DEFINITION |
|---|---|
| ON | NO LIGHT |
| OFF | BLUE LIGHT |



**SW2: POWER On/Off Switch**

| PIN | DEFINITION | PIN | DEFINITION |
|---|---|---|---|
| 1 | AT/ATX | 16 | GND |
| 2 | DELAY_SETUP | 15 | GND |
| 3 | ON_TIME_0 | 14 | GND |
| 4 | ON_TIME_1 | 13 | GND |
| 5 | OFF_TIME_0 | 12 | GND |
| 6 | OFF_TIME_1 | 11 | GND |
| 7 | STACK0 | 10 | GND |
| 8 | STACK1 | 9 | GND |




**SW2: switch setting**

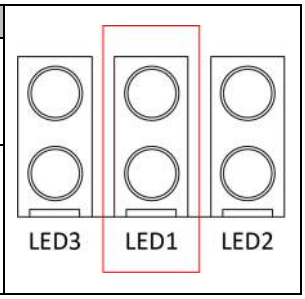
| Power on mode | PIN1 |
|---|---|
| AT | switch to left |
| ATX | switch to right |

| | PIN2 |
|---|---|
| Delay on/off (AT mode) | switch to right: enable |
| | switch to left: disable |

| ON TIME | PIN3 | PIN4 | OFF TIME | PIN5 | PIN6 |
|---|---|---|---|---|---|
| 4 S | 0 | 0 | 30 S | 0 | 0 |
| 8 S | 0 | 1 | 45 S | 0 | 1 |
| 12 S | 1 | 0 | 60 S | 1 | 0 |
| 16 S | 1 | 1 | 90 S | 1 | 1 |
| 0= switch to right<br>1= switch to left | | | | | |

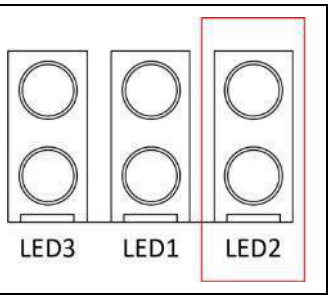
### 2.5 LED Indicator

**LED1: LAN1 LED STATUS**

| LED1 | Light | Dark | Flash | |
|---|---|---|---|---|
| RED | 1000M | 100M | NA |  |
| GREEN | LINK | UNLINK | ACTIVITY | |

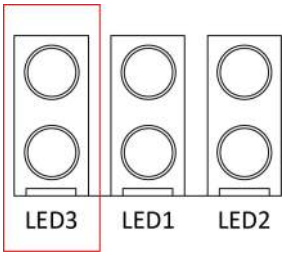


**LED2: LAN2 LED STATUS**

| LED2 | Light | Dark | Flash | |
|---|---|---|---|---|
| RED | 1000M | 100M | NA |  |
| GREEN | Link | Un-link | Activity | |



**LED3: POWER/HDD LED**

| LED2 | Light | Dark | Flash | |
|---|---|---|---|---|
| RED | NA | HDD un-access | HDD access |  |
| GREEN | Power On | Power Off | NA | |

# Chapter 3: Getting Started

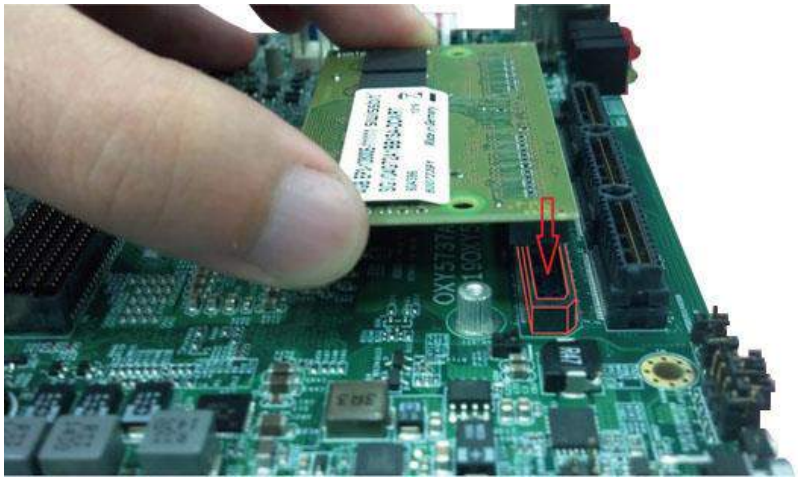
## 3.1 Installing System Memory

The OXY5737A supports 1 x DDR3 1600 XR-DIMM up to 8 GB with ECC (Top Side)

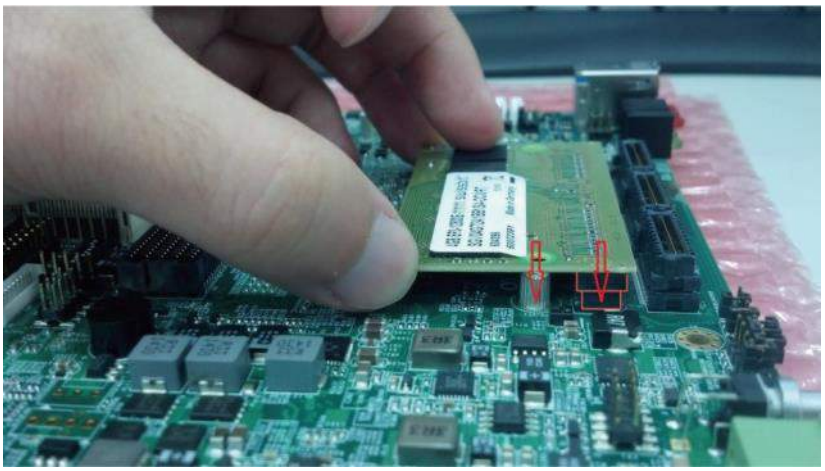
**Disconnect all power supplies to the board before installing a memory module to prevent damage to the board and memory module.**

To install a memory module:

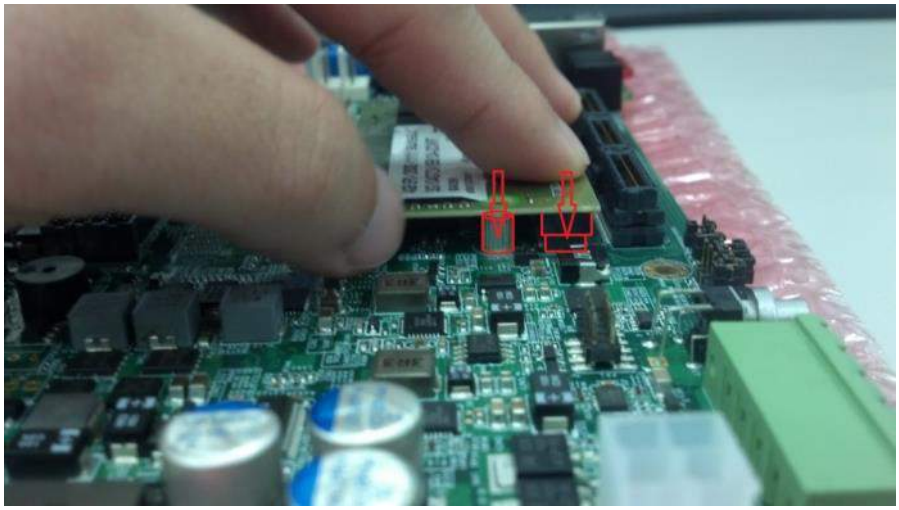
1. Located the memory module slots on the motherboard.



2. Align the memory module with the socket to make sure the notch aligns with the slot key on the socket.



3. Insert the module firmly into the desired slot until the slot lock and secure the memory module.



4. After insert the module to the desire slot, drive screws tighten with memory module's crew hole and bolt on PCB board.

## Chapter 4: AMI BIOS UTILITY

This chapter provides users with detailed descriptions on how to set up a basic system configuration through the AMI BIOS setup utility.

### 4.1 Starting

To enter the setup screens, perform the following steps:

- Turn on the computer and press the <Del> key immediately.
- After the <Del> key is pressed, the main BIOS setup menu displays. Other setup screens can be accessed from the main BIOS setup menu, such as the Chipset and Power menus.

### 4.2 Navigation Keys

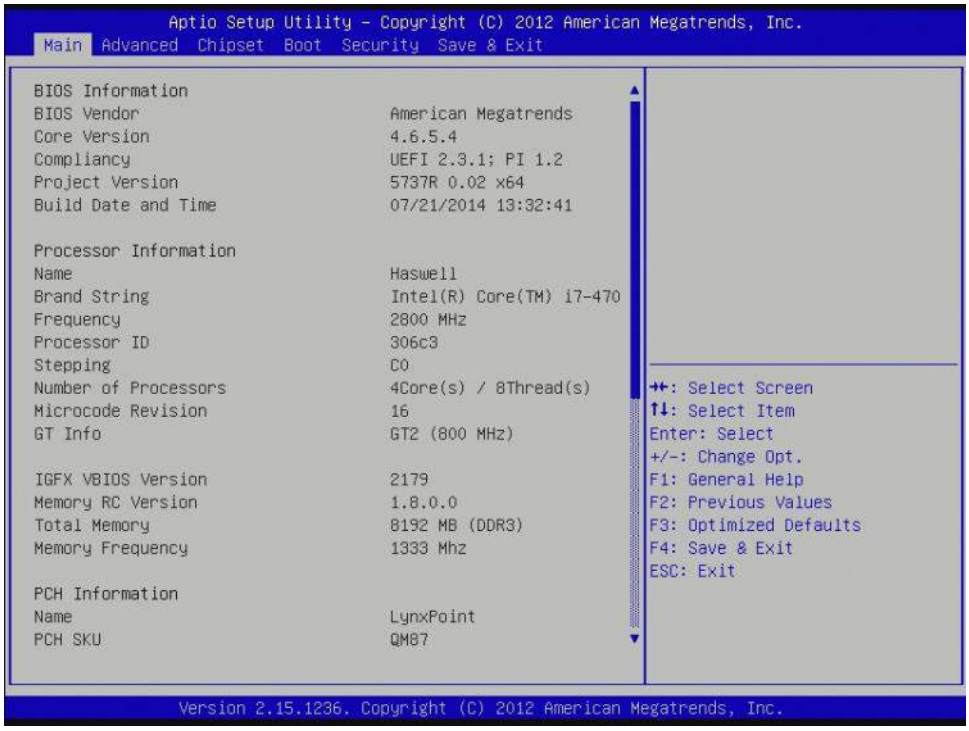
The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.
Some of the hot keys are <F1>, <F10>, <Enter>, <ESC>, and <Arrow> keys.

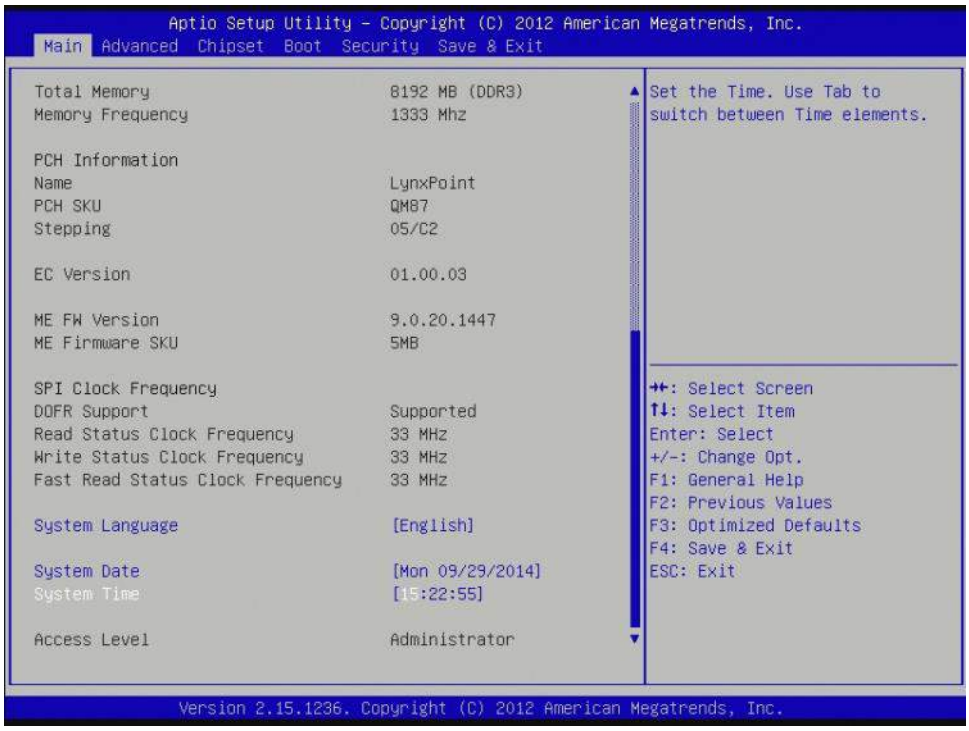
**Some of the navigation keys may differ from one screen to another.**

| | |
|---|---|
| Left/Right | The Left and Right <Arrow> keys moves the cursor to select a menu. |
| Up/Down | The Up and Down <Arrow> keys moves the cursor to select a setup screen or sub-screen. |
| +– Plus/Minus | The Plus and Minus <Arrow> keys changes the field value of a particular setup setting. |
| Tab | The <Tab> key selects the setup fields. |
| F1 | The <F1> key displays the General Help screen. |
| F10 | The <F10> key saves any changes made and exits the BIOS setup utility. |
| Esc | The <Esc> key discards any changes made and exits the BIOS setup utility. |
| Enter | The <Enter> key displays a sub-screen or changes a selected or highlighted option in each menu. |

### 4.3 Main Menu

The Main menu is the screen that first displays when BIOS Setup is entered, unless an error has occurred.




You could setup these items on the Main menu:

**System Language:** Choose the system default language.

**System Date:** Set the date. Use Tab to switch between date elements.

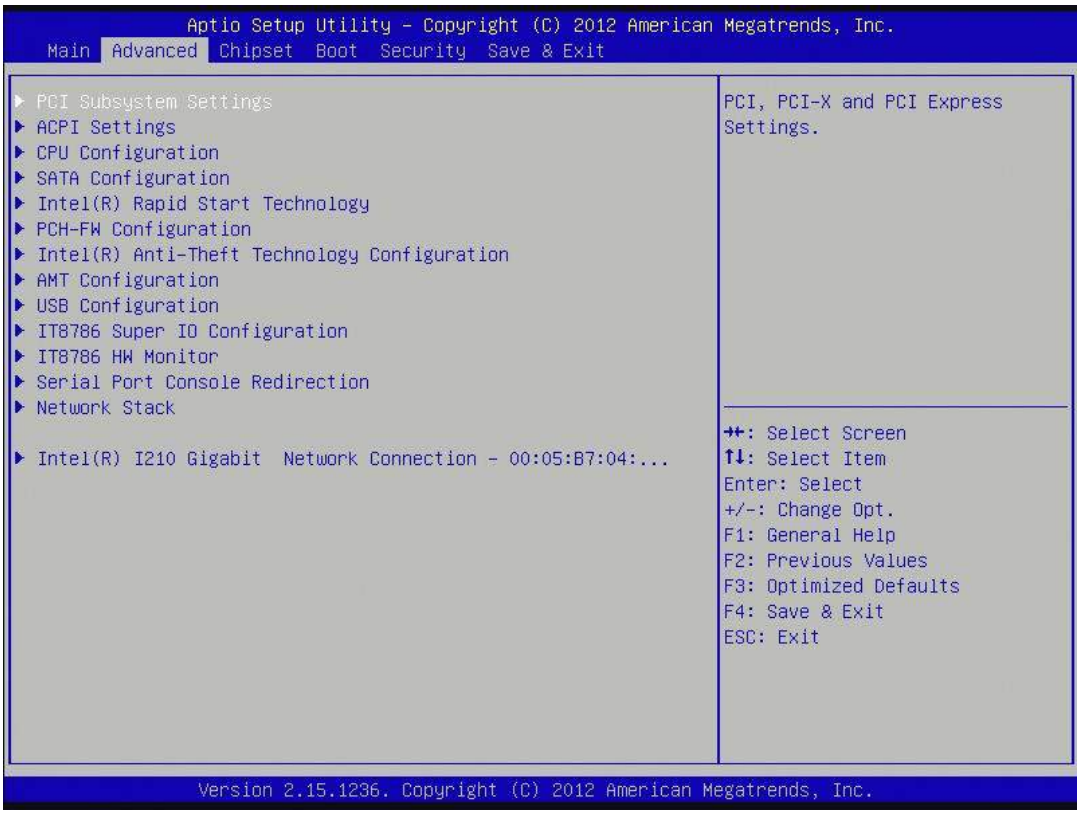
**System Time:** Set the time. Use Tab to switch between time elements.

**Access Level**

Displays the access level of the current user in the BIOS.

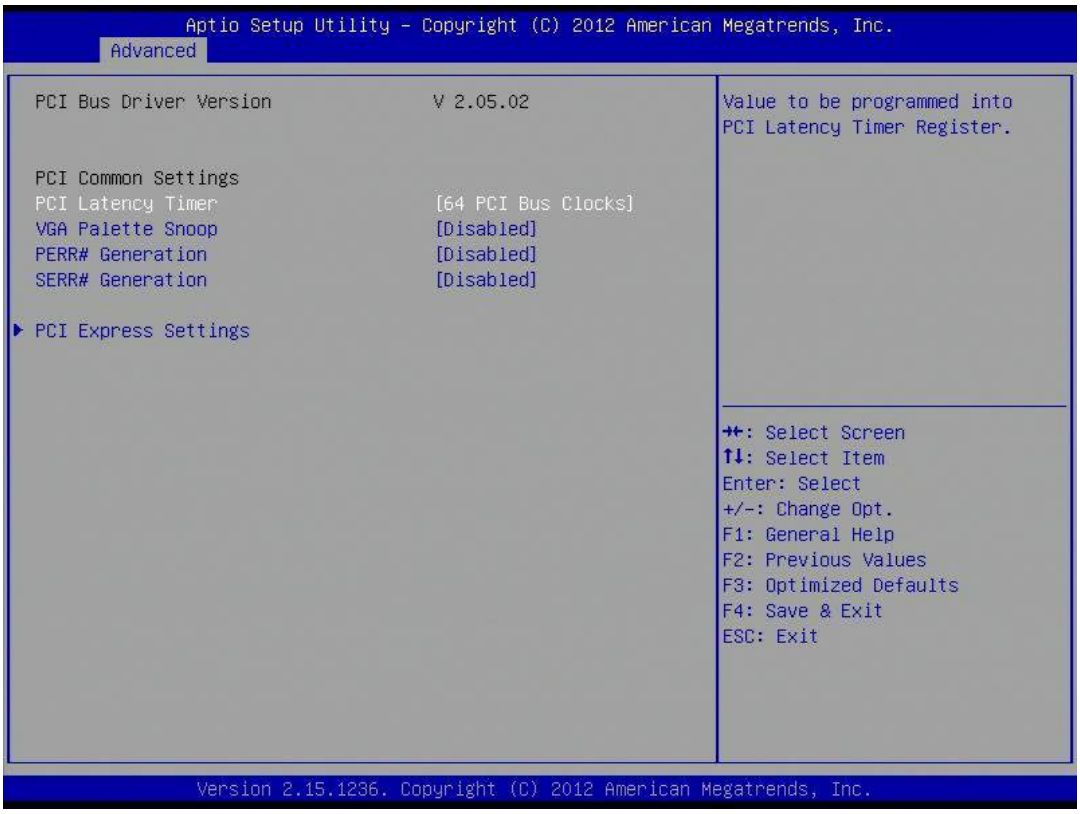
### 4.4 Advanced Menu

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



### 4.4.1 PCI Subsystem Settings

PCI, PCI-X and PCI Express settings.




**PCI Common Settings**

**PCI Latency Timer:** Value to be programed into PCI Latency Timer Register.

**VGA Palette Snoop:** Enable or disable VGA Palette Registers Snooping.

**PERR# Generation:** Enables or Disables PCI Device to Generate PERR#.

**SERR# Generation:** Enables or Disables PCI Device to Generate SERR#.

**PCI Express Settings**

Change PCI Express Devices Settings.

**PCI Express Device Register Settings**

**Relaxed Ordering:** Enables or Disables PCI Express Device Relaxed Ordering.

**Extended Tag:** If ENABLED allows Device to use 8-bit Tag field as a requester.

**No Snoop:** Enabled or Disables PCI Express Device No Snoop option.

**Maximum Payload:** Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

**Maximum Read Request:** Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select value.

**PCI Express Link Register Settings**

**ASPM Support:** Set the ASPM level: Force L0s - Force all links to L0s state: AUTO - BIOS auto configure: DISABLE- Disables ASPM. **WARNING:** Enabling ASPM may cause some PCI-E devices to fail.

**Extended Synch:** If ENBLED allows generation of extended synchronization patterns.

**Link Training Retry**

Defines number of retry attempts software will take to retrain the link if previous training attempt was unsuccessful.

**Link Training Time out (uS)**

Defines number of Microseconds software will wait before polling "Link training" bit in link status register. Value range from 10 to 10000 uS.

**Unpopulated Links**

In order to save power, software will disable unpopulated PCI Express Links. If this option save to "Disable Link".

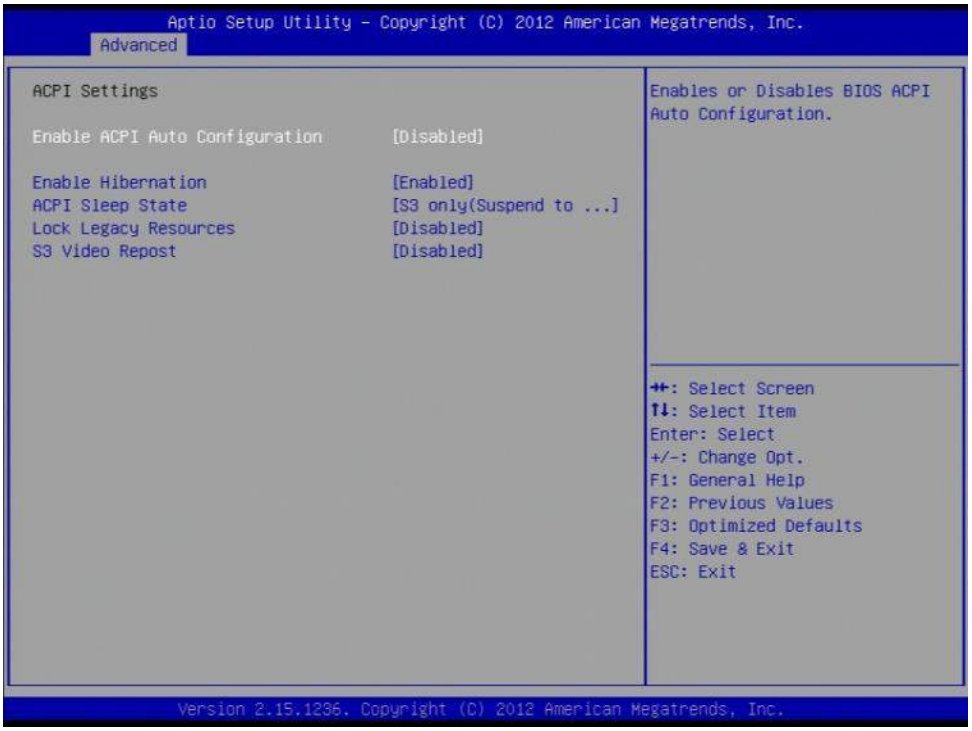
**Restore PCIE Registers**

On non-PCI Express aware OS's some device may not be correctly reinitial after S3. Enableling this restore PCI Express device configurations on S3 resume.

Warning: Enabling this may cause issues with other hardware after S3 resume.

### 4.4.2 ACPI Settings

System ACPI Parameters.




**Enable ACPI Auto Configuration**

Enable/disable BIOS ACPI Auto Configuration.

**Enable Hibernation**

Enables or Disables system ability to hibernate (OS/S4 sleep state). This option may be not effective with some OS.

**ACPI Sleep State**

Select ACPI sleep state the system will enter when the suspend button is pressed.

**Lock Legacy Resources**

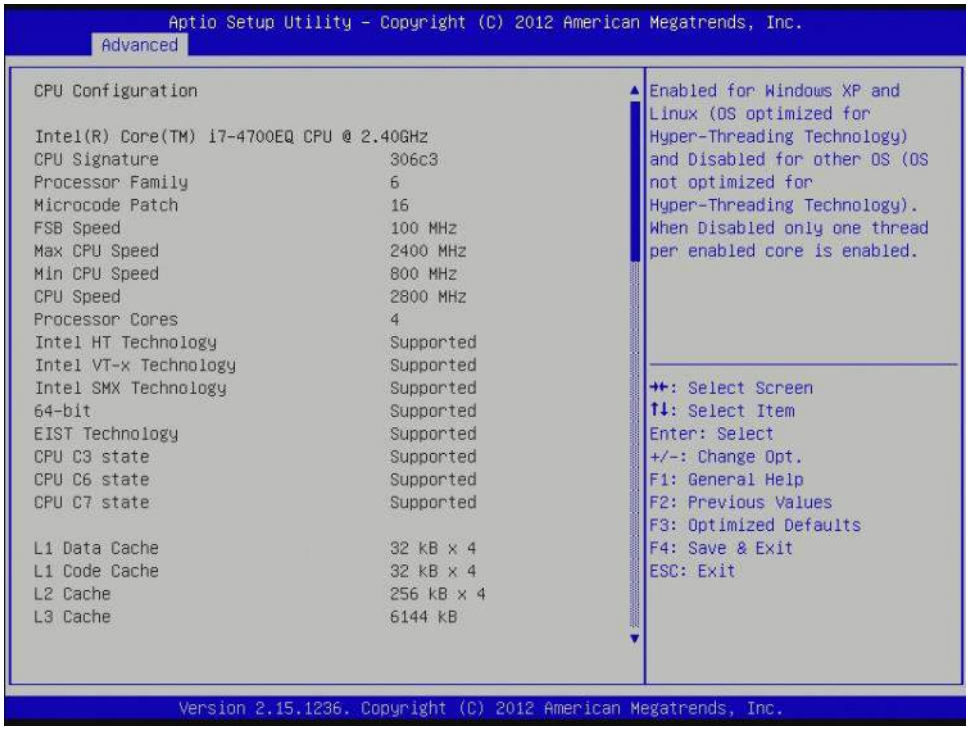
Enable or disable lock of legacy resource.

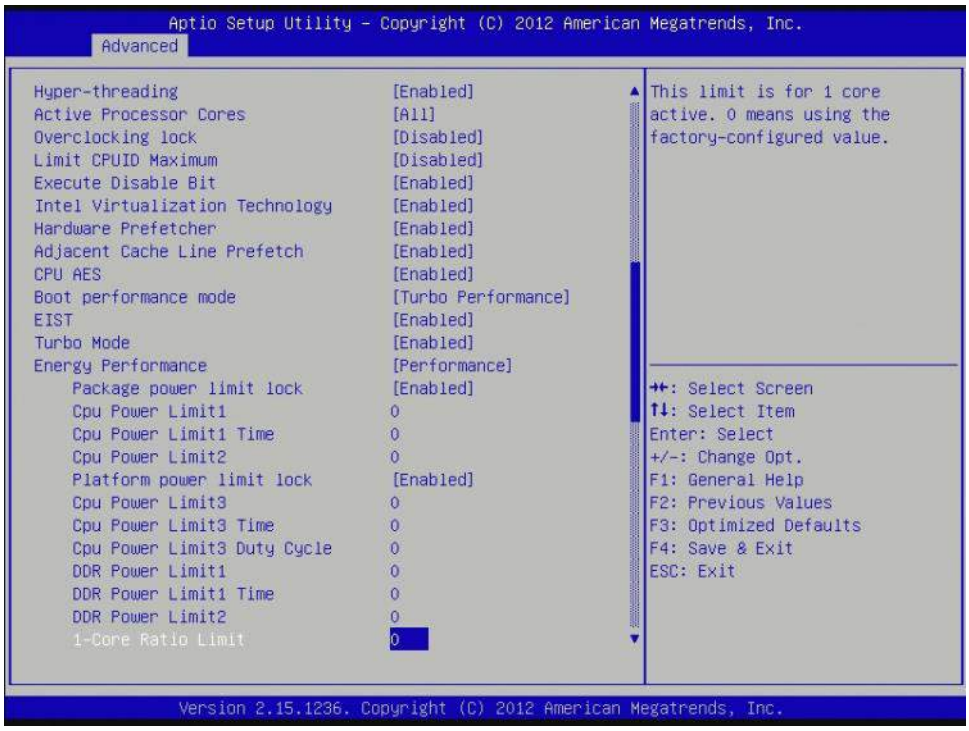
**S3 Video Repost**

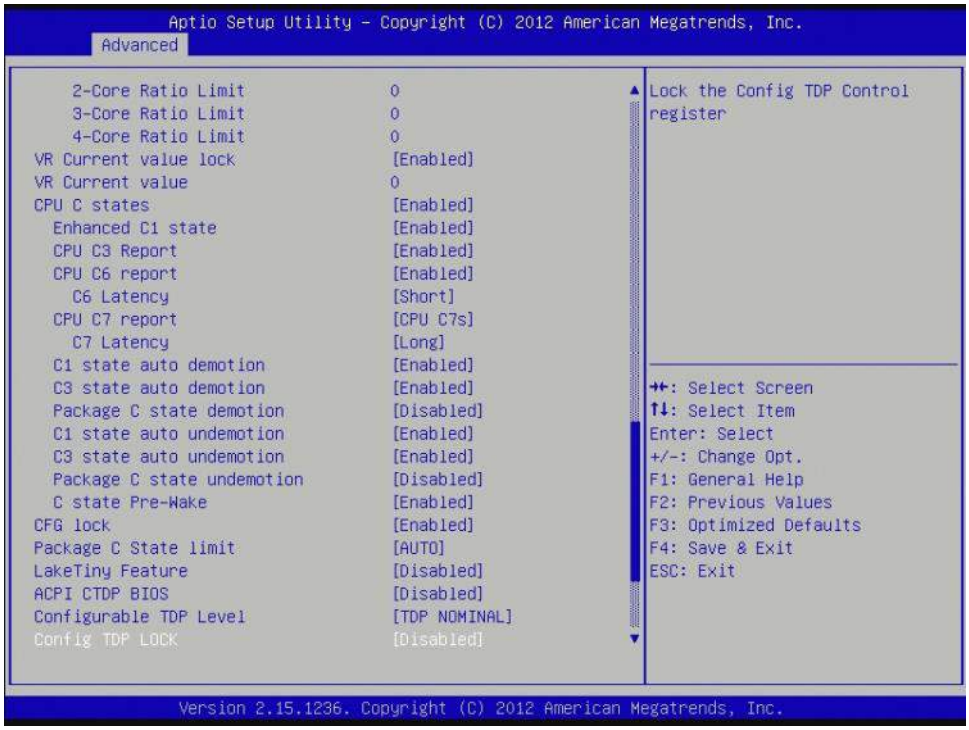
Enable or disable S3 Video Repost.

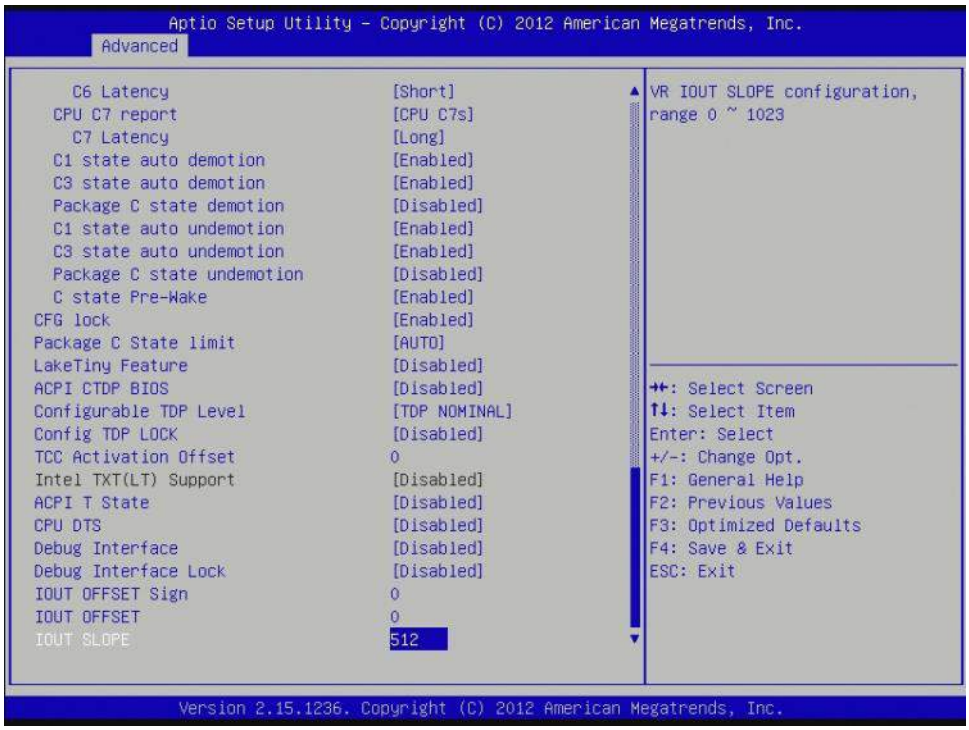
### 4.4.3 CPU configuration

CPU Configuration Parameters.






**Hyper-threading**

Enable for windows XP and Linux(OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.

**Active Processor Cores**

Number of cores to enable in each processor package.

**Overclocking lock**

FLEX_RATIO(194) MSR.

**Limit CPUID Maximum**

Disable for Windows XP.

**Execute Disable Bit**

XD can prevent certain classes of malicious buffer overflow attecks when combined with a supporting OS.

**Intel Virtualization Technology**

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

**Hardware Prefetcher**

Enable the mid level cache(L2) streamer prefetcher.

**Adjacent Cache Line Prefetcher**

Enable the mid level cache(L2) prefetching of adjacent cache lines.

**CPU AES**

Enable/disable CPU advanced encryption standard instruction.

**Boot performance mode**

Select the performance state that the BIOS will set before OS handoff.

**EIST**

Enable/Disable Intel speed step.

**Turbo Mode**

Enable/Disable CPU turbo mode

**Energy performance**

Optimize between performance and power savings.

**Package power limit lock:** When enabled PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.

**CPU Power limit1:** CPU power limit1 value

**CPU Power limit1 time:** Time window which the power limit1 is maintained

**CPU Power limit2:** CPU power limit2 value

**Platform power limit lock:** When enable, PLATFORM_POWER_LIMIT MSD will be locked and a reset will be required to unlock the register.

**CPU Power Limit3:** CPU Power Limit3 value

**CPU Power Limit3 Time:** Time window which the power limit3 is maintained

**CPU Power Limit3 Duty Cycle:** Specify the duty cycle in percentage that the CPU is required to maintain over the configured Power Limit3 time windows.

**DDR Power Limit1:** DDR Power limit1 value

**DDR Power Limit1 Time:** Time window which the DDR Power Limit1 is maintained.

**DDR Power Limit2:** DDR Power limit2 value

**1-Core Ratio Limit:** This limit is for 1 core active. 0 means using the factory-configured value.

**2-Core Ratio Limit:** This limit is for 2 cores active. 0 means using the factory-configured value.

**3-Core Ratio Limit:** This limit is for 3 cores active. 0 means using the factory-configured value.

**4-Core Ratio Limit:** This limit is for 4 cores active. 0 means using the factory-configured value.

**VR Current value lock**

Locks VR Current value from further writes until a reset.

**VR Current value**

Voltage regulator current limit. 0 means AUTO.

**CPU C States**

Enable or disable CPU C states.

**Enhanced C1 State:** Enhanced C1 State

**CPU C3 Report:** Enable /disable CPU C3 report to OS

**CPU C6 Report:** Enable /disable CPU C6 report to OS

**C6 Latency:** Configure short/long latency for C6

**CPU C7 Report:** Enable /disable CPU C7 report to OS

**C7 Latency:** Configure short/long latency for C7

**C1 state auto demotion:** processor will conditionally demote C3/C6/C7 requests to C1 based on uncore auto-demote information.

**C3 state auto demotion:** processor will conditionally demote C6/C7 requests to C3 based on uncore

auto-demote information.

**Package C state demotion:** enable package C state demotion

**C1 state auto undemotion:** undemotion from demoted C1.

**C3 state auto undemotion:** undemotion from demoted C1.

**Package C state undemotion:** enable package C state undemotion

**C state Pre-wake:** Enable or disable C state Pre-Wake feature.

**CFG lock**

Configure MSR 0xE2[15], CFG lock bit.

**Package C State limit**

C0/C1, C2, C3, C6, C7, C7s, AUTO

**LakeTiny Feature**

Enable/Disable LakeTiny for C state configuration.

**ACPI CTDP BIOS**

Enable/Disable ACPI CTDP BIOS support.

**Configurable TDP level**

Allows reconfiguration of TDP levels base on current power and thermal delivery capabilities of the system.

**Configure TDP lock**

Lock the Config TDP control register.

**TCC activation offset**

Offset from the factory TCC activation temperature.

**Intel TXT(LT) Support**

Only Disable

**ACPI T state**

Enable/Disable ACPI T state support.

**CPU DTS**

Disabled: ACPI thermal management uses EC reported temperature value.

Enabled: ACPI thermal management uses DTS SMM mechanism to obtain CPU temperature values.

Out of Spec: ACPI Thermal Management uses EC reported temperature values and DTS SMM is used to handle Out of spec.

**Debug interface**

Enable/Disable CPU debug feature.

**Debug interface lock**

Lock CPU debug interface setting.

**IOUT OFFSET Sign**

0 positive offset. 1 negative offset.

**IOUT OFFSET**

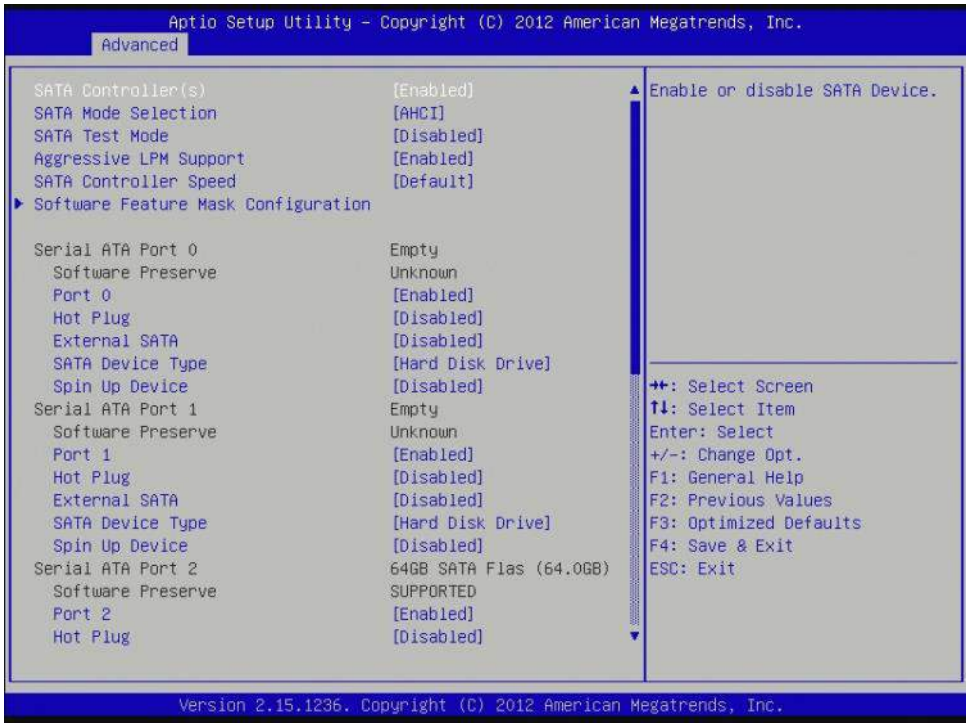
VR IOUT OFFSET configuration 0~625.

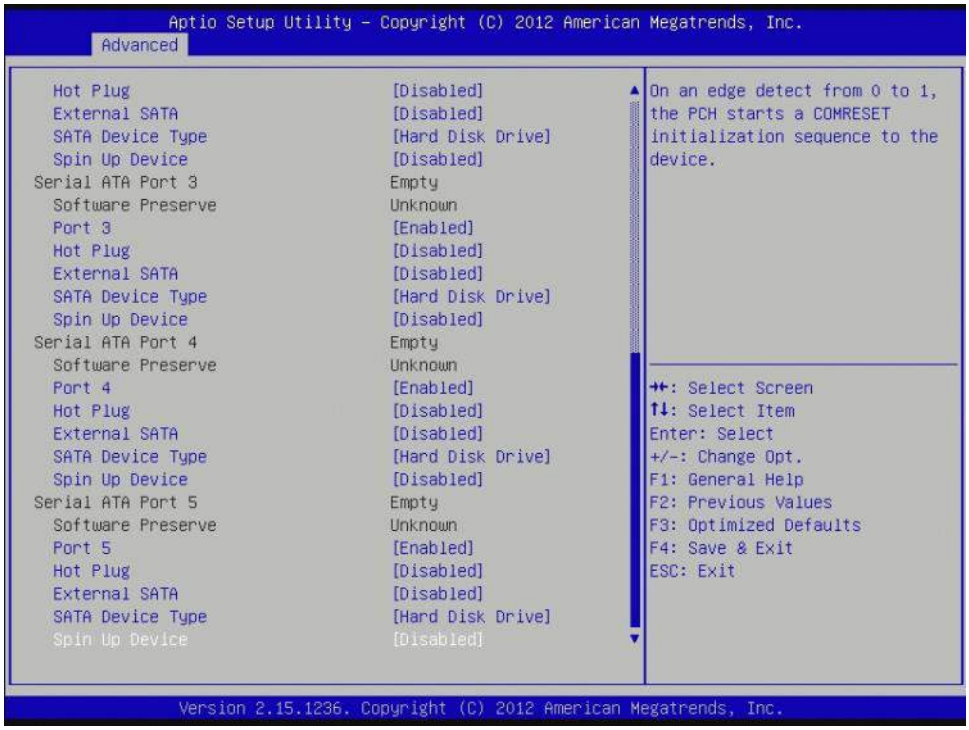
**IOUT SLOPE**

VR IOUT SLOPE configuration range 0~1023.

### 4.4.4 SATA Configuration

This section is used to configure the SATA drives.






**SATA Controller(s)**

Enable or disable SATA device.

**SATA Mode Selection**

Determines how SATA controller(s) operate. The options are: IDE, AHCI, RAID

**SATA Test Selection**

Enable or disable Test Mode

**Aggressive LPM Support**

Enable PCH to aggressively enter link power state.

**SATA Controller Speed**

Indicates the maximum speed the SATA controllers can support. The options are default, Gen1, Gen2, Gen3.

**Software Feature Mask Configuration**

RADI OROM/RST driver will refer to the SWFW configuration to enable or disable the storage features.

**RAID0:** Enable or disable RAID0 feature.

**RAID1:** Enable or disable RAID1 feature.

**RAID10:** Enable or disable RAID10 feature.

**RAID5:** Enable or disable RAID5 feature.

**Intel Rapid Recovery Technology:** Enable or disable Intel Rapid Recovery Technology.

**OROM UI and Banner:** If enabled, then the OROM UI is shown. Otherwise, no OROM banner or information will be displayed if all disks and RAID volumes are Normal.

**HDD unlock:** If enabled, indicates that the HDD password unlock in the OS is enabled.

**LED Locate:** If enabled, indicates that the LED/SGPIO hardware is attached and ping yo locate features is enabled on the OS.

**IRRT Only on eSATA:** If enabled, then only IRRT volumes can span internal and eSATA drives. If disabled, then any RAID volume can span internal and eSATA drives.

**Smart Response Technology:** Enabled or disable Smart Response Technology.

**OROM UI Delay:** If enabled, indicates the delay of the OROM UI Splash Screen in a normal status. The options are 2 seconds, 4 seconds, 6 seconds, 8 seconds.

**Serial ATA Port 0**

**Port 0:** Enable or disable SATA port

**Hot Plug:** Designates this port as Hot Pluggable.

**External SATA:** External SATA support.

**SATA device type:** Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

**Spin Up Device:** On an edge detec from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

**Serial ATA Port 1**

**Port 1:** Enable or disable SATA port

**Hot Plug:** Designates this port as Hot Pluggable.

**External SATA:** External SATA support.

**SATA device type:** Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

**Spin Up Device:** On an edge detec from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

**Serial ATA Port 2**

**Port 2:** Enable or disable SATA port

**Hot Plug:** Designates this port as Hot Pluggable.

**External SATA:** External SATA support.

**SATA device type:** Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

**Spin Up Device:** On an edge detec from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

**Serial ATA Port 3**

**Port 3:** Enable or disable SATA port

**Hot Plug:** Designates this port as Hot Pluggable.

**External SATA:** External SATA support.

**SATA device type:** Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

**Spin Up Device:** On an edge detec from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

**Serial ATA Port 4**

**Port 4:** Enable or disable SATA port

**Hot Plug:** Designates this port as Hot Pluggable.

**External SATA:** External SATA support.

**SATA device type:** Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

**Spin Up Device:** On an edge detec from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

**Serial ATA Port 5**

**Port 5:** Enable or disable SATA port

**Hot Plug:** Designates this port as Hot Pluggable.

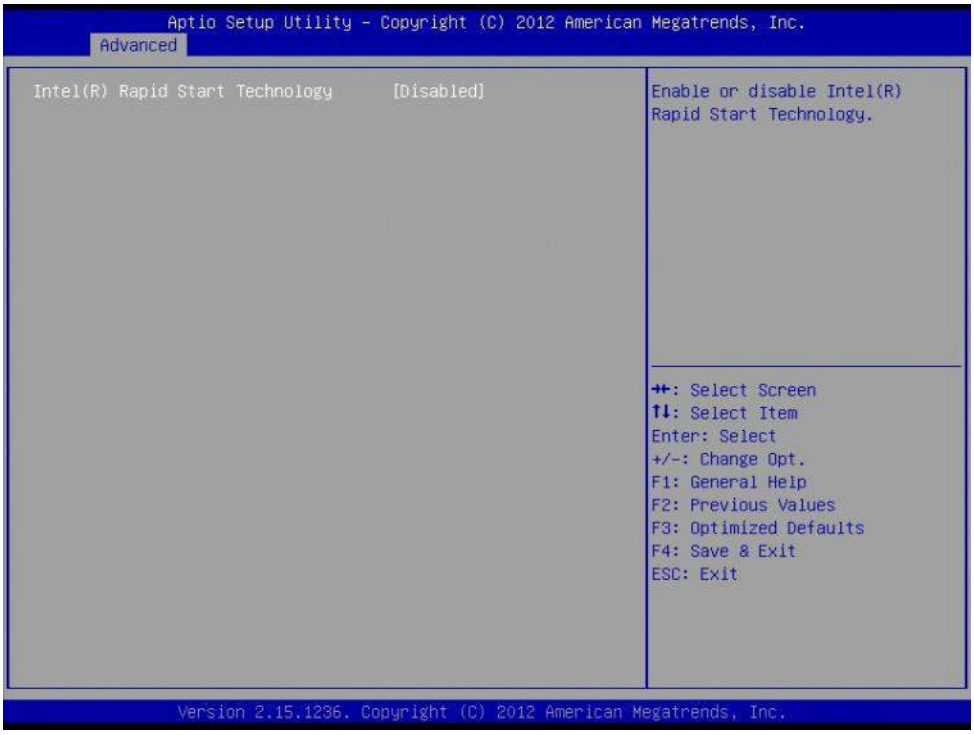
**External SATA:** External SATA support.

**SATA device type:** Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

**Spin Up Device:** On an edge detec from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

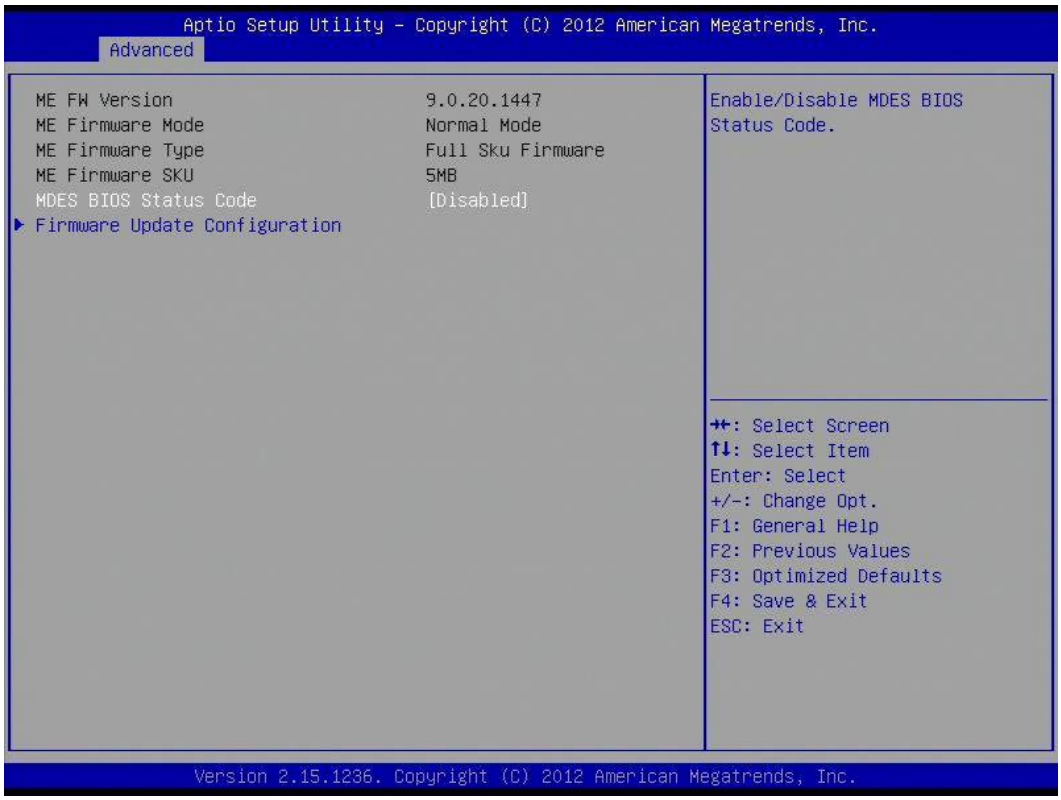
### 4.4.5 Intel Rapid Start Technology

Enable or disable Intel Rapid Start Technology




### 4.4.6 PCH-FW Configuration

Configure Management Engine Technology Parameters.



**MDES BIOS Status Code**

Enable/Disable MDES BIOS Status Code.

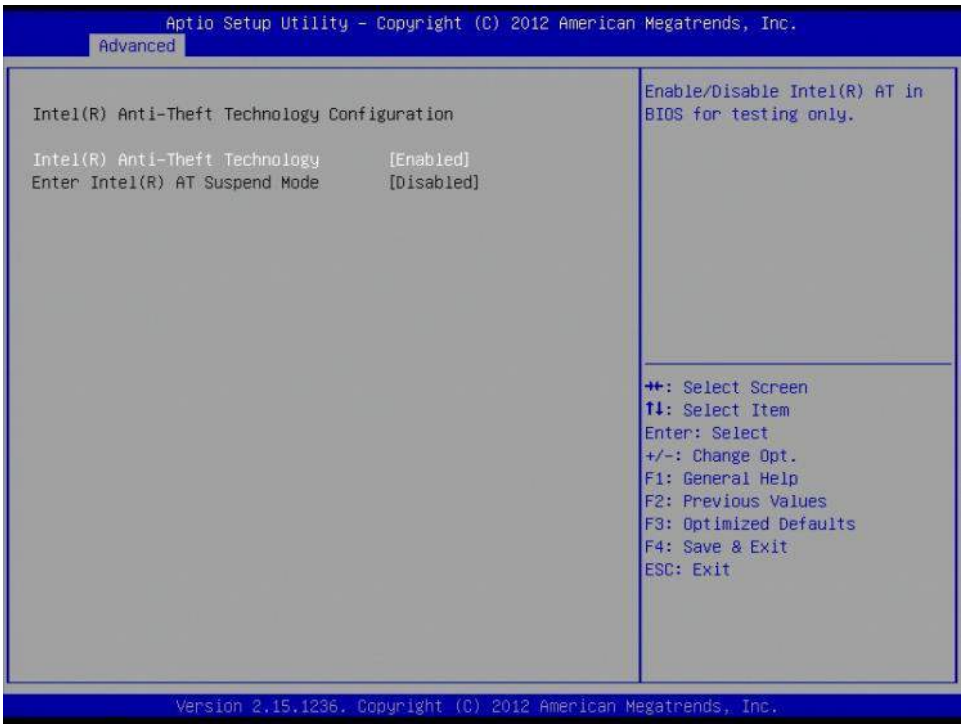
**Firmware Update Configuration**

Configure Management Engine Technology Parameters.

**Me FW Image Re-Flash:** Enable/Disable Me FW Image Re-Flash function.

### 4.4.7 Intel Anti-Theft Technology Configuration

Disabling Intel AT allow user to login to platform. This is strictly for testing only. This does not disable Intel AT services in ME.




**Intel Anti-Theft Technology**

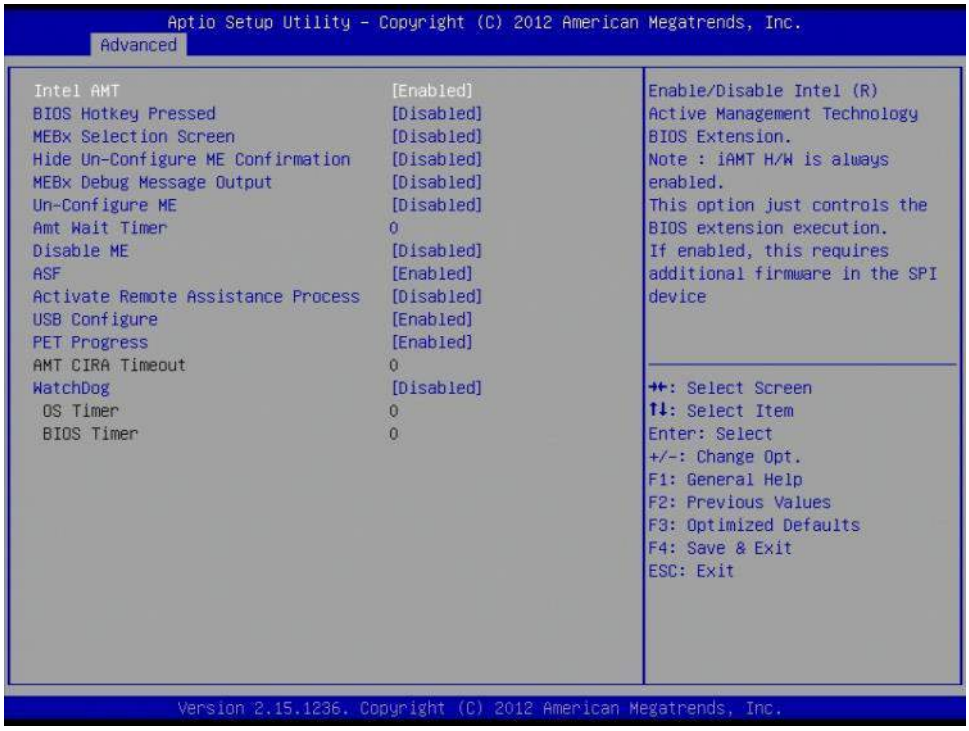
Enable/Disable Intel AT in BIOS for testing. On

**Enter Intel AT Suspend Mode**

Only Disabled

### 4.4.8 AMT Configuration

Configure Active Management Technology Parameters.




**Intel AMT**

Enable/Disable Intel Active Management Technology BIOS Extension.

Note: iAMT H/W is always enabled.

This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

**BIOS Hotkey Pressed**

OEMFlag Bit 1: Enable/Disable BIOS hotkey press.

**MEBx Selection Screen**

OEMFlag Bit 2: Enable/Disable MEBx selection screen.

**Hide Un-Configure ME Confirmation**

OEMFlag Bit 6: Hide Un-Configure ME without password Configuration prompt.

**MEBx Debug Message Output**

OEMFlag Bit 14: Enable MEBx debug message output.

**Un-Configure ME**

OEMFlag Bit 15: Un-Configure ME without password.

**Amt Wait Timer**

Set Timer to wait before sending ASF_GET_BOOT_OPTIONS.

**Disable ME**

Set ME to Soft Temporary Disabled.

**ASF**

Enable/Disable Alert Specification Format.

**Activate Remote Assistance Process**

Trigger CIRA boot.

**USB Configure**

Enable/Disable USB Configure function.

**PET Progress**

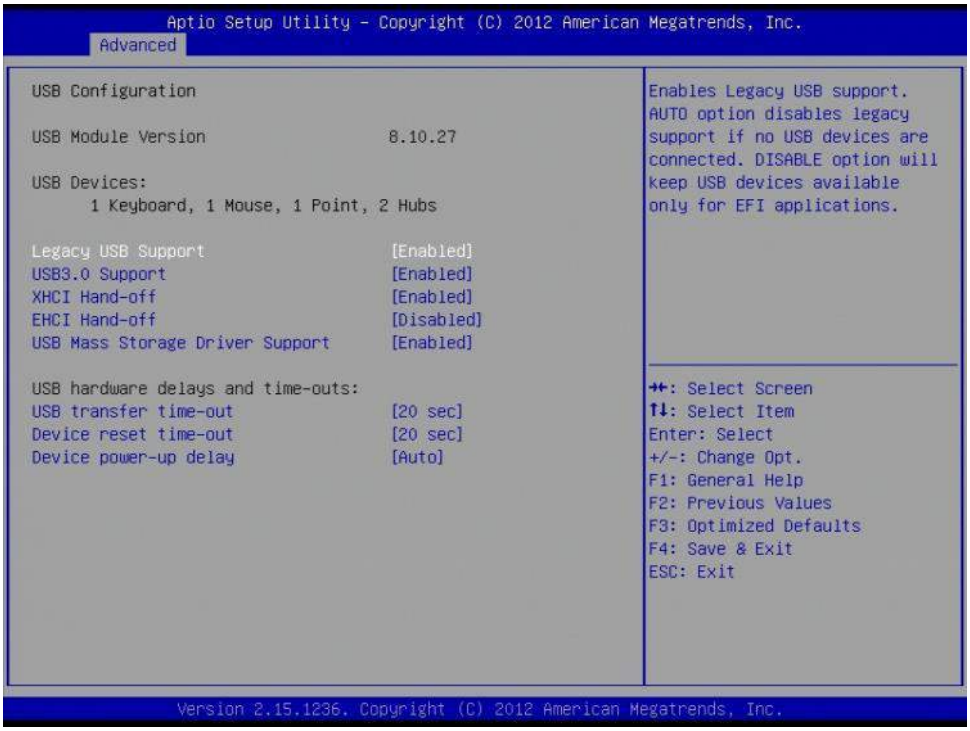
User can Enable/Disable PET Events progress to receive PET events or not.

**WatchDog**

Enable/Disable WatchDog Timer.

### 4.4.9 USB Configuration

USB Configuration Parameters.




**Legacy USB Support**

Enables legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

**USB3.0 Support**

Enable/Disable USB3.0 (XHCI) Controller support.

**XHCI Hand-off**

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

**EHCI Hand-off**

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

**USB Mass Storage Driver Support**

Enable/Disable USB Mass Storage Driver Support.

**USB hardware delays and time-outs:**

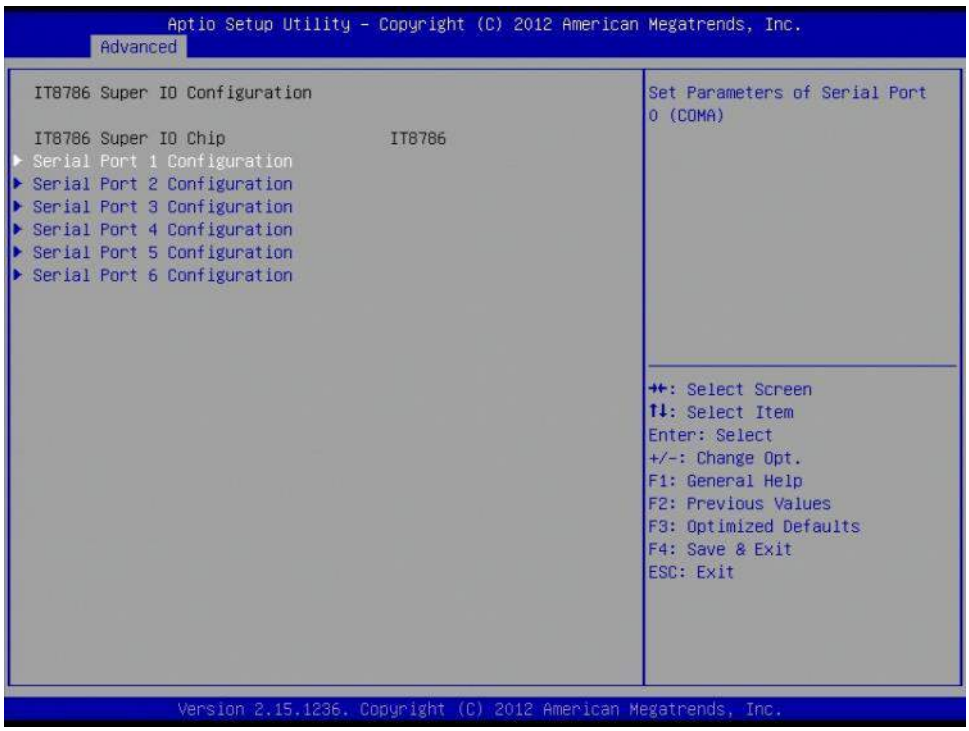
**USB transfer time-out:** The time-out value for Control, Bulk, and Interrupt transfers. The options are 1 sec, 5 sec, 10 sec, 20 sec.

**Device reset time-out:** USB mass storage device Start Unit command time-out. The options are 10 sec, 20 sec, 30 sec, 40 sec.

**Device power-up delay:** Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Hub port the delay is taken from Hub descriptor. The options are Auto, manual.

### 4.4.10 IT8786 Super IO Configuration

System Super IO Chip Parameters.




**Serial Port 1 Configuration**

Set Parameters of Serial Port 0 (COMA).

**Serial Port:** Enable or Disable Serial Port (COM).

**Device Settings:** IO=3F8h, IRQ=4

**Change Settings:** Select an optimal setting for Super IO device.

**Serial Port 2 Configuration**

Set Parameters of Serial Port 1 (COMB).

**Serial Port:** Enable or Disable Serial Port (COM).

**Device Settings:** IO=2F8h, IRQ=3

**Change Settings:** Select an optimal setting for Super IO device.

**Serial Port 3 Configuration**

Set Parameters of Serial Port 2 (COMC).

**Serial Port:** Enable or Disable Serial Port (COM).

**Device Settings:** IO=3E8h, IRQ=7

**Change Settings:** Select an optimal setting for Super IO device.

**Serial Port 4 Configuration**

Set Parameters of Serial Port 3 (COMD).

**Serial Port:** Enable or Disable Serial Port (COM).

**Device Settings:** IO=2E8h, IRQ=7

**Change Settings:** Select an optimal setting for Super IO device.

**Serial Port 5 Configuration**

Set Parameters of Serial Port 4 (COME).

**Serial Port:** Enable or Disable Serial Port (COM).

**Device Settings:** IO=2F0h, IRQ=7

**Change Settings:** Select an optimal setting for Super IO device.

**Serial Port 6 Configuration**

Set Parameters of Serial Port 5 (COMF).

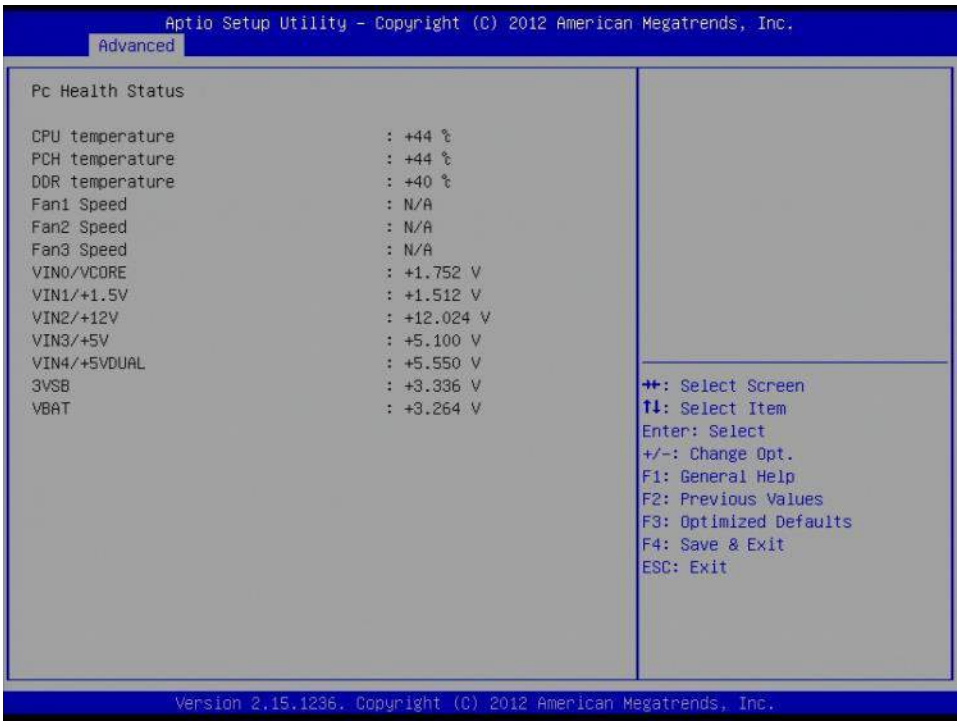
**Serial Port:** Enable or Disable Serial Port (COM).

**Device Settings:** IO=2E0h, IRQ=7

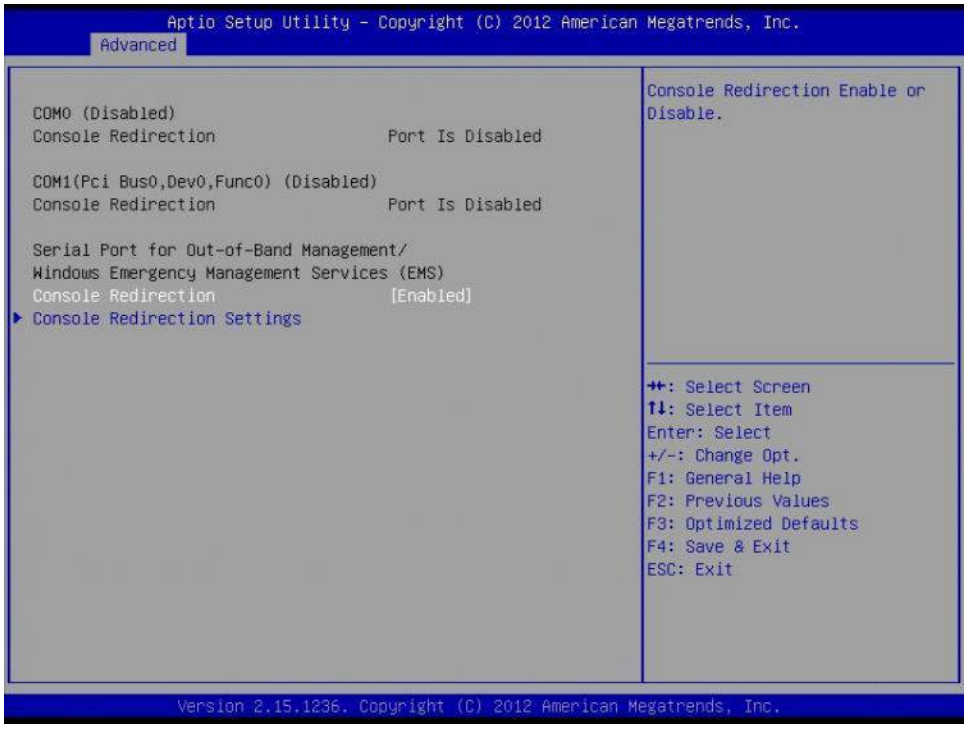
**Change Settings:** Select an optimal setting for Super IO device.

### 4.4.11 IT8786 HW Monitor

Monitor hardware status.




### 4.4.12 Serial Port Console Redirection




**Console Redirection**

Console Redirection Enable or Disable.

**Console Redirection Setting**

The Settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible setting.

**Out-of-Band Mgmt Port:** Microsoft Windows Emergency Management Service allows for remote management of a Windows Server OS through a serial port. The options are COM0 (Disabled), COM1(Pci Bus0, Dev0, Func0) (Disabled)

**Terminal Type:** VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation. The options are VT100, VT100+, VT-UTF8, ANSI.

**Bits per second:** selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds. The options are 9600, 19200, 57600, 115200.

**Flow Control:** Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "star" signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. The options are None, Hardware RTS/CTS, Software Xon/xoff

**Data bits:** 8

**Parity:** None

**Stop bits:** 1

### 4.4.13 Network Stack

Network stack settings

**Network Stack**

Enable/Disable UEFI network stack

### 4.4.14 Intel I210-IT Gigabit Network Connection

Configure Gigabit Ethernet device parameters.


**PORT CONFIGURATION MENU**

**NIC Configuration:** Configure Boot Protocol, wake on LAN, Link Speed, and VLAN.

**Blink LEDs:** Identify the physical network port by blinking the associated LED.

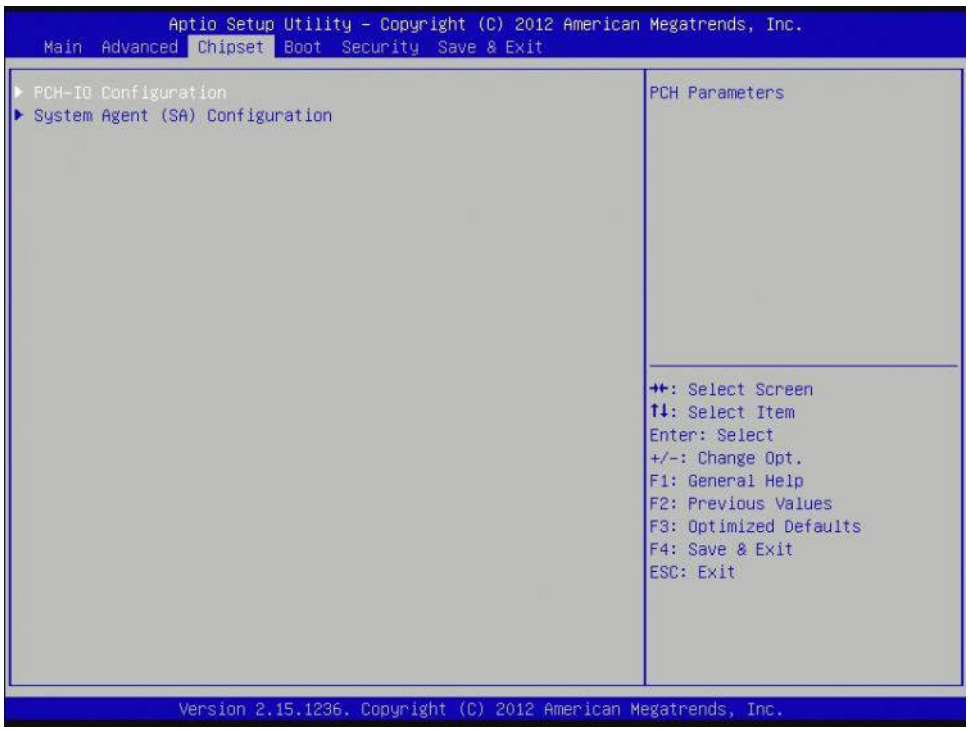
**PORT CONFIGURATION INFORMATION**

**Link Status:** Link Status.

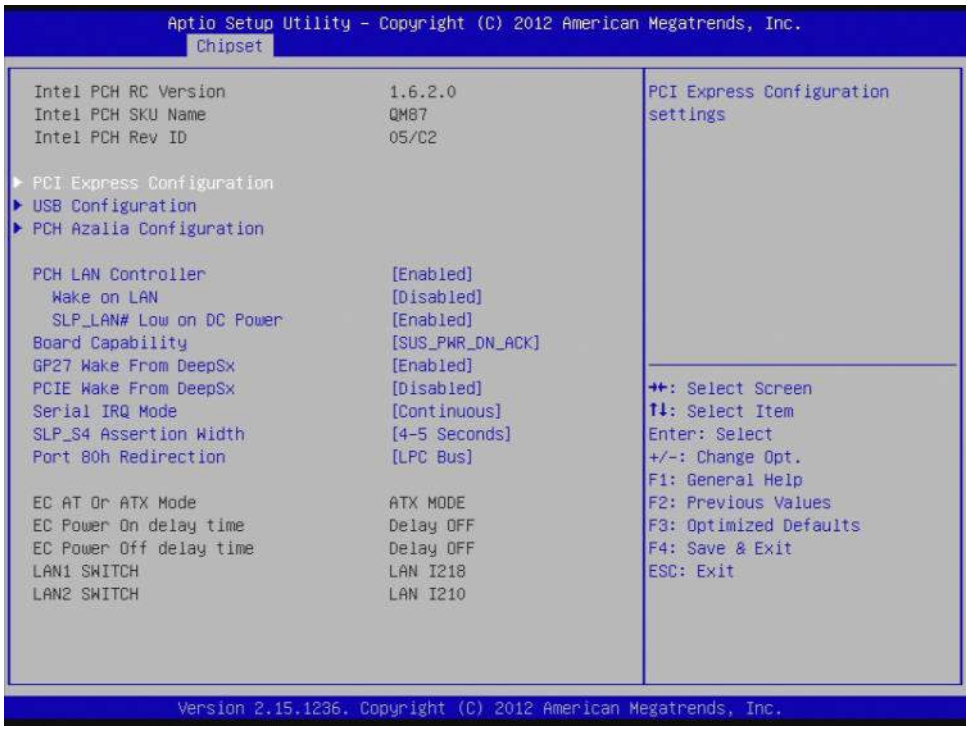
**Virtual MAC Address:** Programmatically assignable MAC address for port.

### 4.5 Chipset

This section gives you functions to configure the system based on the specific features of the chipset. The chipset manages bus speeds and access to system memory resources.




#### 4.5.1 PCH IO configuration



**PCI Express Configuration**

PCI Express Configuration settings

**PCIE Root Port Function Swapping:** Enable or disable PCI Express PCI Express Root Port Function Swapping.

**Subtractive Decode:** Enable or disable PCI Express Subtractive Decode.

**PCI Express Root Port1**

PCI Express Root Port1 setting. Only enabled

**ASPM Support:** Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure : DISABLE – Disables ASPM. The options are Disabled, L0s, L1, L0SL1, Auto

**L1 Substates:** PCI Express L1 Substates setting. The options are Disabled, L1.1, L1.2, L1.1 & L1.2

**URR:** Enable or disable PCI Express Unsupported Request Reporting.

**FER:** Enable or disable PCI Express Device Fatal Error Reporting.

**NFER:** Enable or disable PCI Express Device Non-Fatal Error Reporting.

**CER:** Enable or disable PCI Express Device Correctable Error Reporting.

**CTO:** Enable or disable PCI Express Completion Timer TO.

**SEFE:** Enable or disable Root PCI Express System Error on Fatal Error.

**SENFE:** Enable or disable Root PCI Express System Error on Non-Fatal Error.

**SECE:** Enable or disable Root PCI Express System Error on Correctable Error.

**PME SCI:** Enable or disable PCI Express PME SCI.

**Hot Plug:** Enable or disable PCI Express Hot Plug.

**PCIe Speed:** Select PCI Express port speed.

**Detect Non-Compliance Device:** Detect Non Compliance PCI Express Device. If enable, it will take more time at POST time.

**Extra Bus Reserved:** Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

**Reseved Memory:** Reserved Memory Range for this Root Bridge.

**Prefetchable Memory:** Prefetchable Memory Range for this Root Bridge.

**Reserved I/O:** Reserved I/O (4K/8K/12K/16K/…/48K) Range for this Root Bridge.

**PCIE LTR:** PCIE Latency Reporting Enable/Disable.

**PCIE LTR Lock:** PCIE LTR configuration lock.

**Snoop Latency Ocerride:** Snoop Latency Ocerride for PCH PCIE.

**Non Snoop Latency Ocerride:** Non Snoop Latency Ocerride for PCH PCIE.

**PCI Express Root Port2**

control the PCI Express Root port, the options are enabled/disabled.

**ASPM Support:** Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

**L1 Substates:** PCI Express L1 Substates setting.

**URR:** Enable or disable PCI Express Unsupported Request Reporting.

**FER:** Enable or disable PCI Express Device Fatal Error Reporting.

**NFER:** Enable or disable PCI Express Device Non-Fatal Error Reporting.

**CER:** Enable or disable PCI Express Device Correctable Error Reporting.

**CTO:** Enable or disable PCI Express Completion Timer TO.

**SEFE:** Enable or disable Root PCI Express System Error on Fatal Error.

**SENFE:** Enable or disable Root PCI Express System Error on Non-Fatal Error.

**SECE:** Enable or disable Root PCI Express System Error on Correctable Error.

**PME SCI:** Enable or disable PCI Express PME SCI.

**Hot Plug:** Enable or disable PCI Express Hot Plug.

**PCIe Speed:** Select PCI Express port speed.

**Detect Non-Compliance Device:** Detect Non Compliance PCI Express Device. If enable, it will take more time at POST time.

**Extra Bus Reserved:** Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

**Reseved Memory:** Reserved Memory Range for this Root Bridge.

**Prefetchable Memory:** Prefetchable Memory Range for this Root Bridge.

**Reserved I/O:** Reserved I/O (4K/8K/12K/16K/…/48K) Range for this Root Bridge.

**PCIE LTR:** PCIE Latency Reporting Enable/Disable.

**PCIE LTR Lock:** PCIE LTR configuration lock.

**Snoop Latency Ocerride:** Snoop Latency Ocerride for PCH PCIE.

**Non Snoop Latency Ocerride:** Non Snoop Latency Ocerride for PCH PCIE.

**PCI Express Root Port3**

control the PCI Express Root port, the options are enabled/disabled

**ASPM Support:** Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

**L1 Substates:** PCI Express L1 Substates setting.

**URR:** Enable or disable PCI Express Unsupported Request Reporting.

**FER:** Enable or disable PCI Express Device Fatal Error Reporting.

**NFER:** Enable or disable PCI Express Device Non-Fatal Error Reporting.

**CER:** Enable or disable PCI Express Device Correctable Error Reporting.

**CTO:** Enable or disable PCI Express Completion Timer TO.

**SEFE:** Enable or disable Root PCI Express System Error on Fatal Error.

**SENFE:** Enable or disable Root PCI Express System Error on Non-Fatal Error.

**SECE:** Enable or disable Root PCI Express System Error on Correctable Error.

**PME SCI:** Enable or disable PCI Express PME SCI.

**Hot Plug:** Enable or disable PCI Express Hot Plug.

**PCIe Speed:** Select PCI Express port speed.

**Detect Non-Compliance Device:** Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.

**Extra Bus Reserved:** Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

**Reseved Memory:** Reserved Memory Range for this Root Bridge.

**Prefetchable Memory:** Prefetchable Memory Range for this Root Bridge.

**Reserved I/O:** Reserved I/O (4K/8K/12K/16K/…/48K) Range for this Root Bridge.

**PCIE LTR:** PCIE Latency Reporting Enable/Disable.

**PCIE LTR Lock:** PCIE LTR Configuration Lock.

**Snoop Latency Ocerride:** Snoop Latency Ocerride for PCH PCIE.

**Non Snoop Latency Ocerride:** Non Snoop Latency Ocerride for PCH PCIE.

**PCI Port 4 is assigned to LAN**

**PCI Express Root Port5:**

control the PCI Express Root port, the options are enabled/disabled

**ASPM Support:** Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

**L1 Substates:** PCI Express L1 Substates setting.

**URR:** Enable or disable PCI Express Unsupported Request Reporting.

**FER:** Enable or disable PCI Express Device Fatal Error Reporting.

**NFER:** Enable or disable PCI Express Device Non-Fatal Error Reporting.

**CER:** Enable or disable PCI Express Device Correctable Error Reporting.

**CTO:** Enable or disable PCI Express Completion Timer TO.

**SEFE:** Enable or disable Root PCI Express System Error on Fatal Error.

**SENFE:** Enable or disable Root PCI Express System Error on Non-Fatal Error.

**SECE:** Enable or disable Root PCI Express System Error on Correctable Error.

**PME SCI:** Enable or disable PCI Express PME SCI.

**Hot Plug:** Enable or disable PCI Express Hot Plug.

**PCIe Speed:** Select PCI Express port speed.

**Detect Non-Compliance Device:** Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.

**Extra Bus Reserved:** Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

**Reseved Memory:** Reserved Memory Range for this Root Bridge.

**Prefetchable Memory:** Prefetchable Memory Range for this Root Bridge.

**Reserved I/O:** Reserved I/O (4K/8K/12K/16K/…/48K) Range for this Root Bridge.

**PCIE LTR:** PCIE Latency Reporting Enable/Disable.

**PCIE LTR Lock:** PCIE LTR Configuration Lock.

**Snoop Latency Ocerride:** Snoop Latency Ocerride for PCH PCIE.

**Non Snoop Latency Ocerride:** Non Snoop Latency Ocerride for PCH PCIE.

**PCI Express Root Port6**

control the PCI Express Root port, the options are enabled/disabled

**ASPM Support:** Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

**L1 Substates:** PCI Express L1 Substates setting.

**URR:** Enable or disable PCI Express Unsupported Request Reporting.

**FER:** Enable or disable PCI Express Device Fatal Error Reporting.

**NFER:** Enable or disable PCI Express Device Non-Fatal Error Reporting.

**CER:** Enable or disable PCI Express Device Correctable Error Reporting.

**CTO:** Enable or disable PCI Express Completion Timer TO.

**SEFE:** Enable or disable Root PCI Express System Error on Fatal Error.

**SENFE:** Enable or disable Root PCI Express System Error on Non-Fatal Error.

**SECE:** Enable or disable Root PCI Express System Error on Correctable Error.

**PME SCI:** Enable or disable PCI Express PME SCI.

**Hot Plug:** Enable or disable PCI Express Hot Plug.

**PCIe Speed:** Select PCI Express port speed.

**Detect Non-Compliance Device:** Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.

**Extra Bus Reserved:** Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

**Reseved Memory:** Reserved Memory Range for this Root Bridge.

**Prefetchable Memory:** Prefetchable Memory Range for this Root Bridge.

**Reserved I/O:** Reserved I/O (4K/8K/12K/16K/…/48K) Range for this Root Bridge.

**PCIE LTR:** PCIE Latency Reporting Enable/Disable.

**PCIE LTR Lock:** PCIE LTR Configuration Lock.

**Snoop Latency Ocerride:** Snoop Latency Ocerride for PCH PCIE.

**Non Snoop Latency Ocerride:** Non Snoop Latency Ocerride for PCH PCIE.

**PCI Express Root Port7**

control the PCI Express Root port, the options are enabled/disabled

**ASPM Support:** Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

**L1 Substates:** PCI Express L1 Substates setting.

**URR:** Enable or disable PCI Express Unsupported Request Reporting.

**FER:** Enable or disable PCI Express Device Fatal Error Reporting.

**NFER:** Enable or disable PCI Express Device Non-Fatal Error Reporting.

**CER:** Enable or disable PCI Express Device Correctable Error Reporting.

**CTO:** Enable or disable PCI Express Completion Timer TO.

**SEFE:** Enable or disable Root PCI Express System Error on Fatal Error.

**SENFE:** Enable or disable Root PCI Express System Error on Non-Fatal Error.

**SECE:** Enable or disable Root PCI Express System Error on Correctable Error.

**PME SCI:** Enable or disable PCI Express PME SCI.

**Hot Plug:** Enable or disable PCI Express Hot Plug.

**PCIe Speed:** Select PCI Express port speed.

**Detect Non-Compliance Device:** Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.

**Extra Bus Reserved:** Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

**Reseved Memory:** Reserved Memory Range for this Root Bridge.

**Prefetchable Memory:** Prefetchable Memory Range for this Root Bridge.

**Reserved I/O:** Reserved I/O (4K/8K/12K/16K/…/48K) Range for this Root Bridge.

**PCIE LTR:** PCIE Latency Reporting Enable/Disable.

**PCIE LTR Lock:** PCIE LTR Configuration Lock.

**Snoop Latency Ocerride:** Snoop Latency Ocerride for PCH PCIE.

**Non Snoop Latency Ocerride:** Non Snoop Latency Ocerride for PCH PCIE.

**PCI Express Root Port8**

control the PCI Express Root port, the options are enabled/disabled

**ASPM Support:** Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

**L1 Substates:** PCI Express L1 Substates setting.

**URR:** Enable or disable PCI Express Unsupported Request Reporting.

**FER:** Enable or disable PCI Express Device Fatal Error Reporting.

**NFER:** Enable or disable PCI Express Device Non-Fatal Error Reporting.

**CER:** Enable or disable PCI Express Device Correctable Error Reporting.

**CTO:** Enable or disable PCI Express Completion Timer TO.

**SEFE:** Enable or disable Root PCI Express System Error on Fatal Error.

**SENFE:** Enable or disable Root PCI Express System Error on Non-Fatal Error.

**SECE:** Enable or disable Root PCI Express System Error on Correctable Error.

**PME SCI:** Enable or disable PCI Express PME SCI.

**Hot Plug:** Enable or disable PCI Express Hot Plug.

**PCIe Speed:** Select PCI Express port speed.

**Detect Non-Compliance Device:** Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.

**Extra Bus Reserved:** Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

**Reseved Memory:** Reserved Memory Range for this Root Bridge.

**Prefetchable Memory:** Prefetchable Memory Range for this Root Bridge.

**Reserved I/O:** Reserved I/O (4K/8K/12K/16K/…/48K) Range for this Root Bridge.

**PCIE LTR:** PCIE Latency Reporting Enable/Disable.

**PCIE LTR Lock:** PCIE LTR Configuration Lock.

**Snoop Latency Ocerride:** Snoop Latency Ocerride for PCH PCIE.

**Non Snoop Latency Ocerride:** Non Snoop Latency Ocerride for PCH PCIE.

**USB Configuration**

**USB Precondition:** Precondition work on USB host controller and root ports for faster enumeration.

**XHCI Mode:** Mode of operation of xHCI controller.

**BTCG:** Enabling/disabling trunk clock gating.

**USB Ports Per-Port Disable Control:** Control each of the USB ports (0~13) disabling.

**PCH Azalia Configuration.**

**Azalia:** Control Detection of the Azalia device.

Disabled=Azalia will be unconditionally disabled.

Enabled=Azalia will be unconditionally Enabled.

Auto=Azalia will be enabled if present, disabled otherwise.

**Azalia Docking Support:** Enable or disable Azalia Docking Support of Audio Controller.

**Azalia PME:** Enable or disable Power Management capability of Audio Controller.

**PCH LAN Controller**

Enable or disable onboard NIC.

**Wake on LAN:** Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

**SLP_LAN# Low on DC Power:** Enable/Disable SLP_LAN# Low on DC Power.

**Board Capability**

Board Capability-SUS_PWR_DN_ACK->Send Disabled to PCH, DeepSx->Show DeepSx Policies.

**GP27 Wake From DeepSx**

Wake from DeepSx by the assertion of GP27 pin.

**PCIE Wake From DeepSx**

Wake from DeepSx by the assertion of PCIE.

**Serial IRQ Mode**

Configure Serial IRQ Mode.

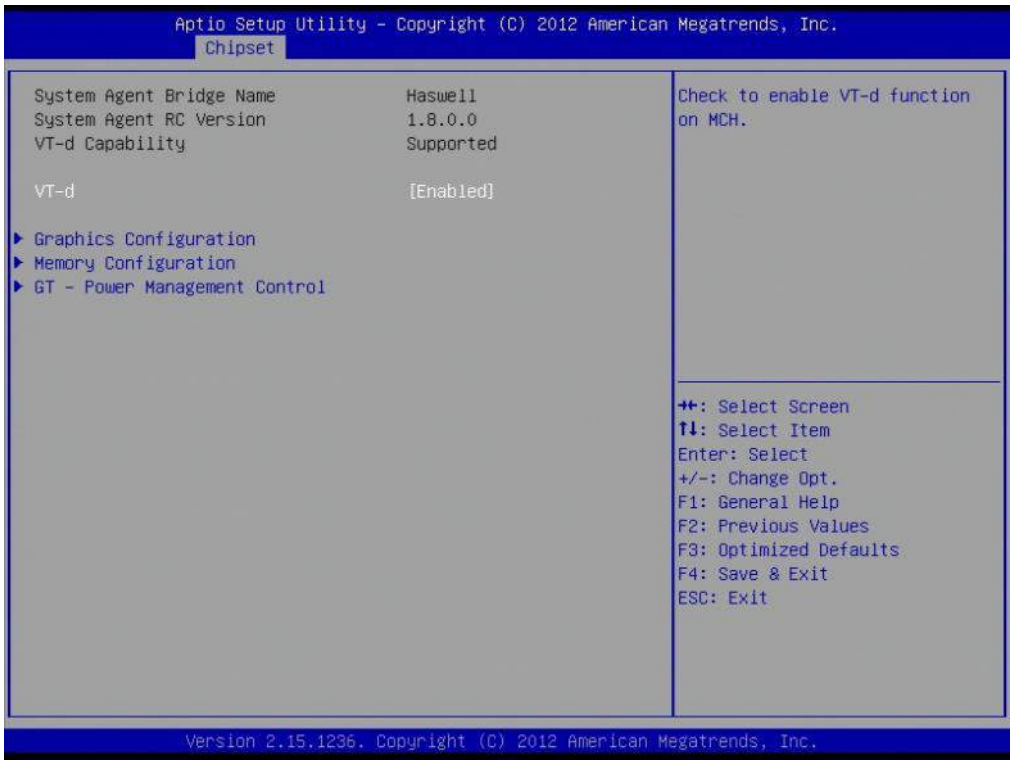
**SLP_S4 Assertion Width**

Select a minimum assertion width of the SLP_S4# signal.

**Port 80h Redirection**

Control where the Port 80h cycles are sent.

### 4.5.2 System AGENT SA




**VT-d**

Check to enable VT-d function on MCH.

**Graphics Configuration**

**Graphics Turbo IMON Current:** Graphics turbo IMON current values supported (14-31).

**Primary Display:** select which of AUTO/IGFX/PEG/SG graphics device should be primary display or select SG for switchable GFX

**Primary PEG:** Select Auto/PEG1/PEG2 Graphics device should be Primary PEG.

**Primary PCIE:** Select Auto/PCIE1/PCIE2/PCIE3/PCIE4PCIE5/PCIE6/PCIE7 Graphics device should be Primary PCIE.

**Internal Graphics:** Keep IGD enabled based on the setup options

**Aperture Size:** Select the Aperture Size.

**DVMT Pre-Allocated:** Select DVMT 5.0 Pre-Allocated (fixed) Graphics memory size used by the internal graphics device.

**DVMT Total Gfx Mem:** Select DVMT5.0 total graphic memory size used by the internal graphics device.

**Gfx Low Power Enable:** this option is applicable for SFF only.

**Panel Power Enable:** Enable/Disable forcing of Panel Power in the BIOS.

**LCD Control**

**Primary IGFX Boot Display:** Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.

**LCD Panel Type:** Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.

**SDVO-LFP Panel Type:** Select SDVO panel used by Internal Graphics Device by selecting the appropriate setup item.

**Panel Scaling:** Select the LCD panel scaling option used by the Internal Graphics Device.

**Backlight control:** backlight control setting

**Panel Color Depth:** select the LFP panel color depth.

**Memory Configuration**

**DIMM profile:** Select DIMM timing profile that should be used.

**Memory Frequency Limiter:** maximum memory frequency selections in Mhz.

**DDR Reset Wait Time:** The value of ns to wait for switch DDR voltage, minimum 20ns.

**ECC Support:** Enable or disable DDR Ecc support

**Max TOLUD:** Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

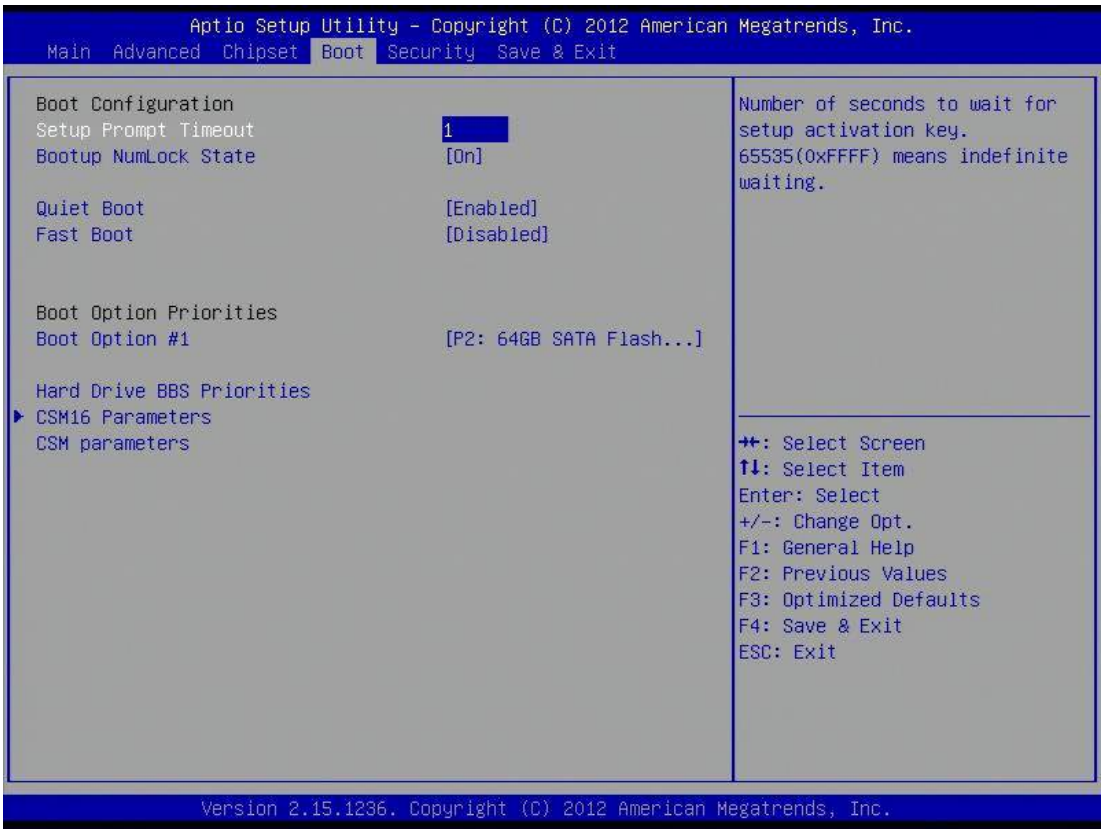
**GT- Power Management Control**

**RC6 (render standby):** check to enable render standby support.

**GT OverClocking Support:** enable or disable GT overclocking support

### 4.6 Boot

This section is used to configure the boot features.




**Setup Prompt Timeout**

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

**Bootup NumLock State**

Select the keyboard NumLock state.

**Quiet Boot**

Enables or disables Quiet Boot option.

**Fast Boot**

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

**Boot option priorities**

**Boot Option #1:** Sets the system boot order.

**Hard Drive BBS Priorities**

Set the order of the legacy devices in this group

**CSM16 Parameters**

Set the order of the legacy devices in this group

**GateA20 Active:** UPON REQUEST – GA20 can be disabled using BIOS serices.ALWAYS-do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

**Option ROM Messages:** Set display mode for option ROM.

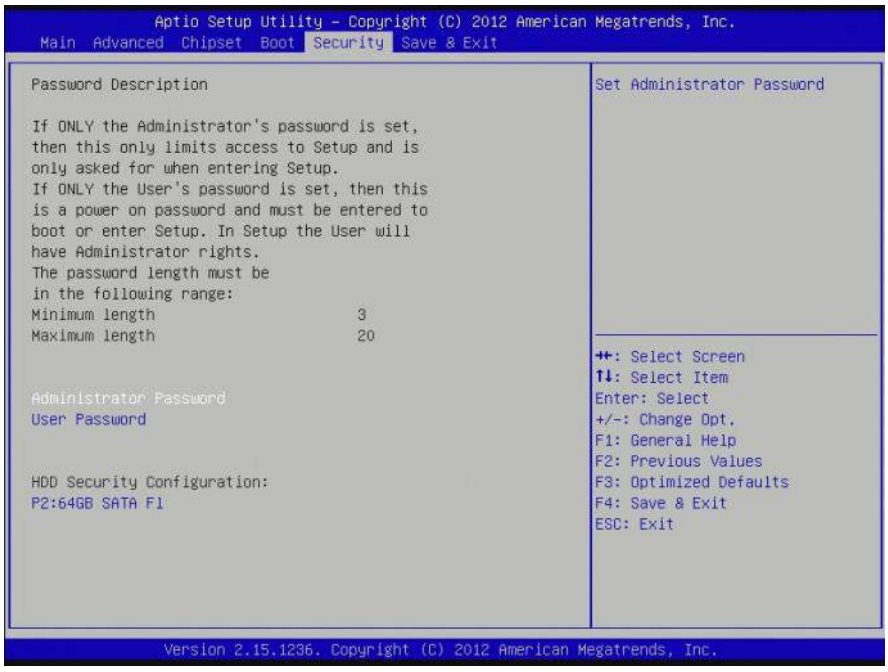
**INT19 Trap Response:** BIOS reaction on INT19 trapping by option ROM: IMMEDIATE-execute the trap right away; POSTPONES-execute the trap during legacy boot.

**CSM Parameters**

OpROM execution, boot options filter, etc.

**4.7 Security**

Use the Security Menu to establish system passwords




**Administrator Password**

Set Administartor Password.

**User Password**

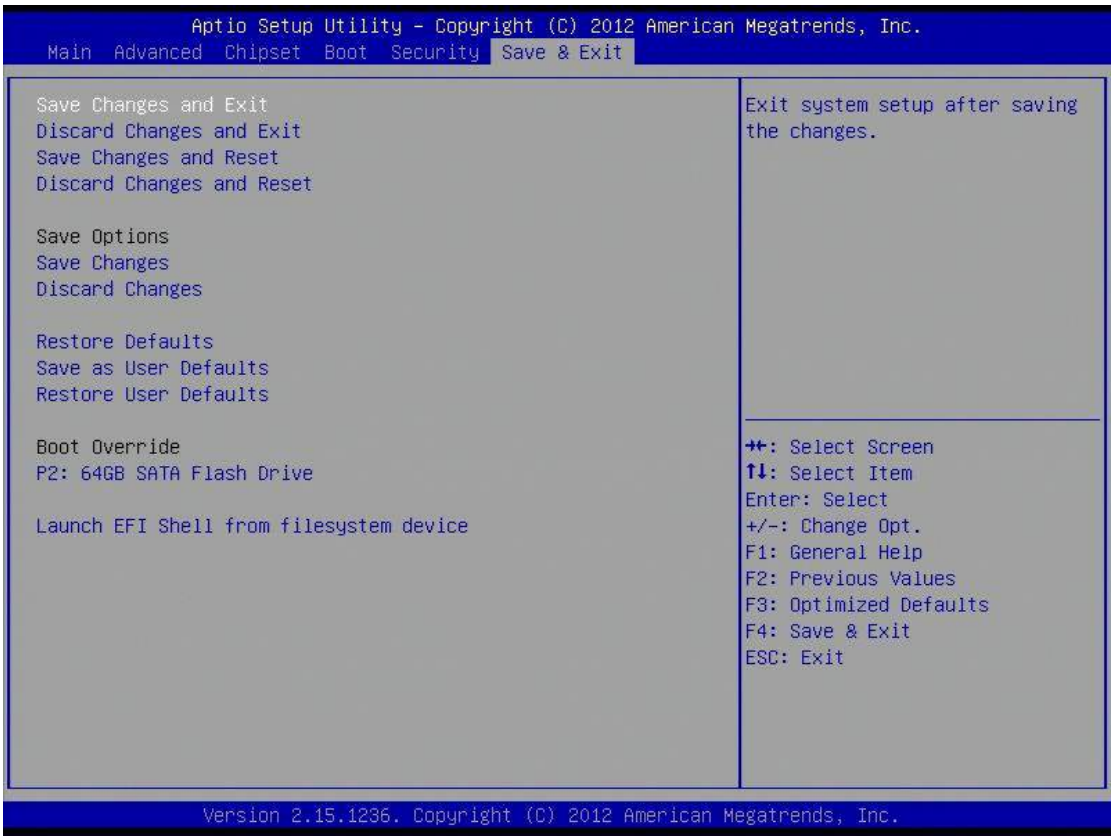
Set User Password.

**HDD Security Configuration**

Set HDD Password.

### 4.8 Save and Exit

This screen provides functions for handling changes made to the BIOS settings and the exiting of the Setup program.




**Save Changes and Exit**

Exit system setup after saving the changes.

**Discard Changes and Exit**

Exit system setup without saving any changes.

**Save Changes and Reset**

Reset the system after saving the changes.

**Discard Changes and Reset**

Reset system setup without saving any changes.

**Save Options**

**Save Changes:** Save Changes done so far to any of the setup options.

**Discard Changes:** Discard Changes done so far to any of the setup options.

**Restore Defaults**

Restore/Load Default values for all the setup options.

**Save as User Defaults**

Save the changes done so far as User Defaults.

**Restore user Defaults**

Restore the User Defaults to all the setup options.

**Launch EFI Shell from filesystem device**

Attempts to launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices.